

FIG. 1

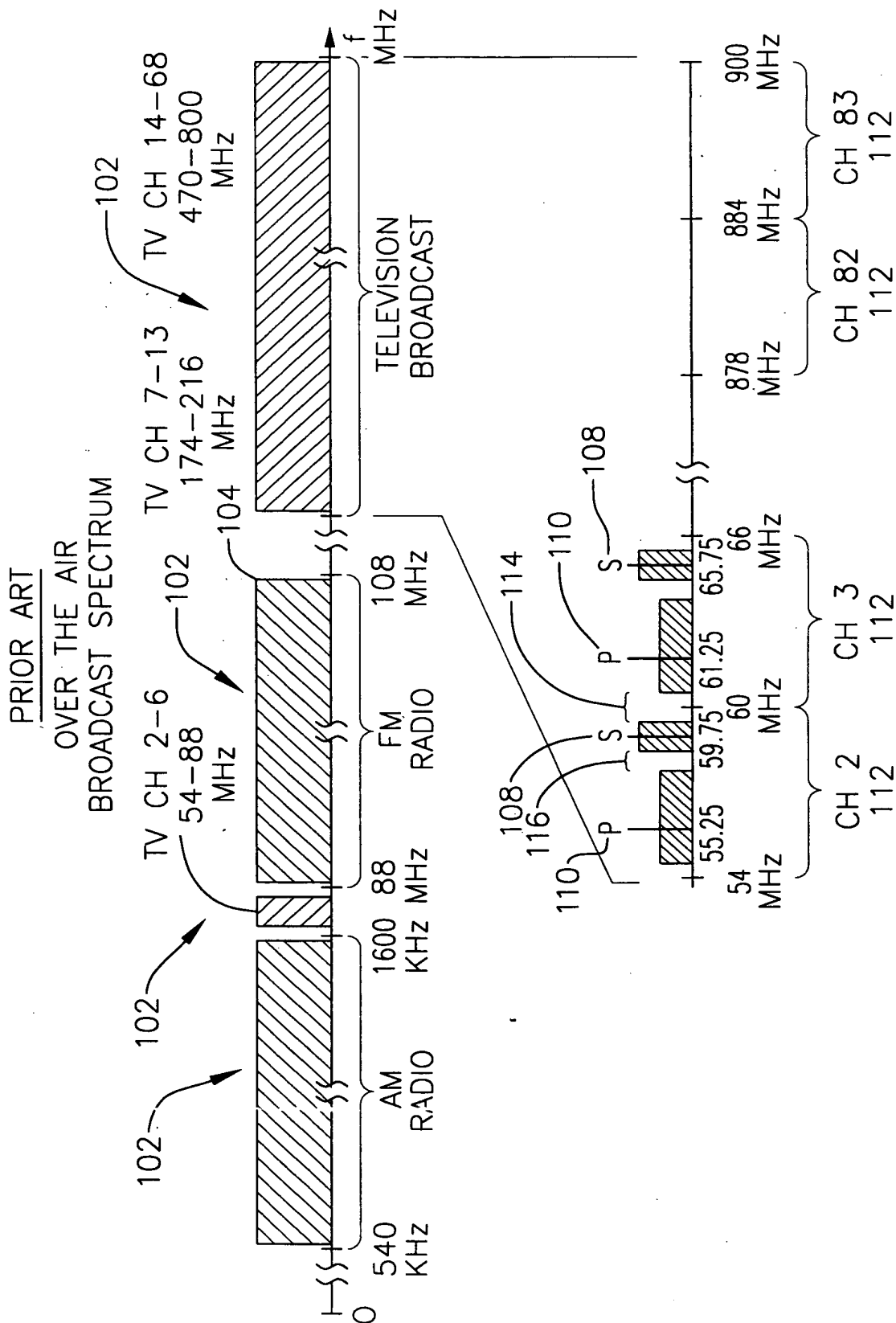


FIG. 2

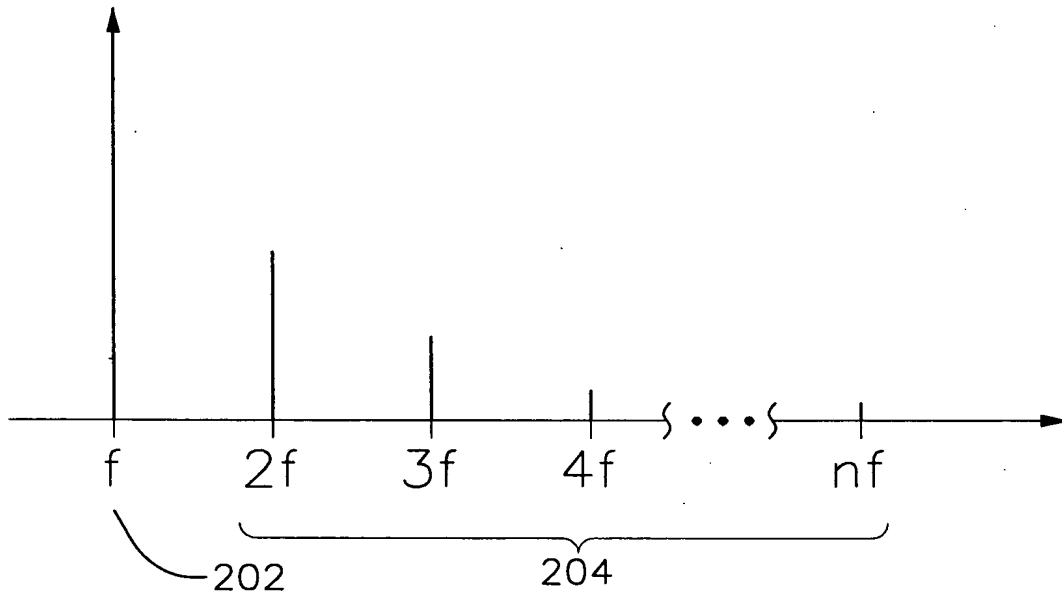


FIG. 3
PRIOR ART

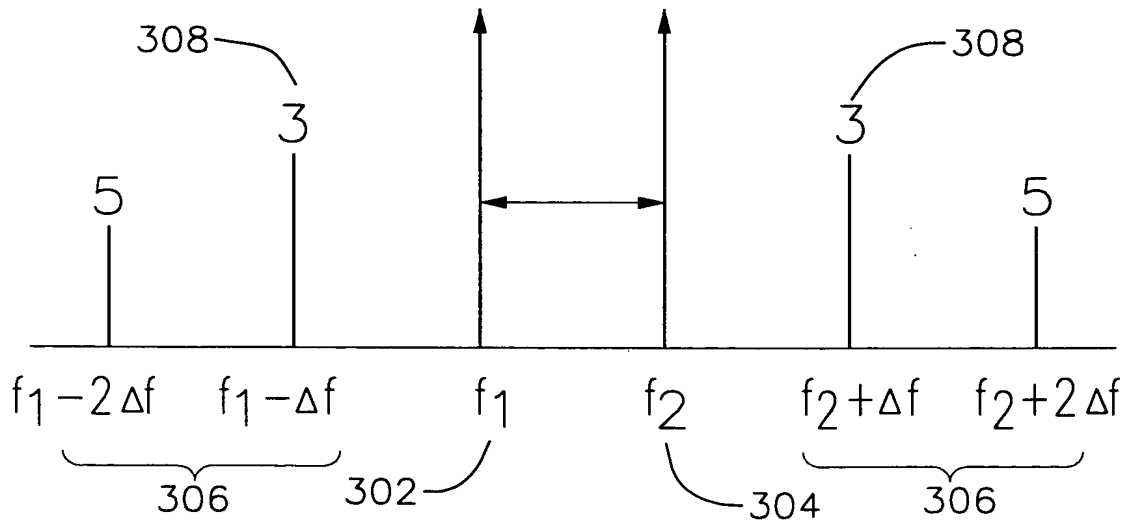


FIG. 4
 PRIOR ART

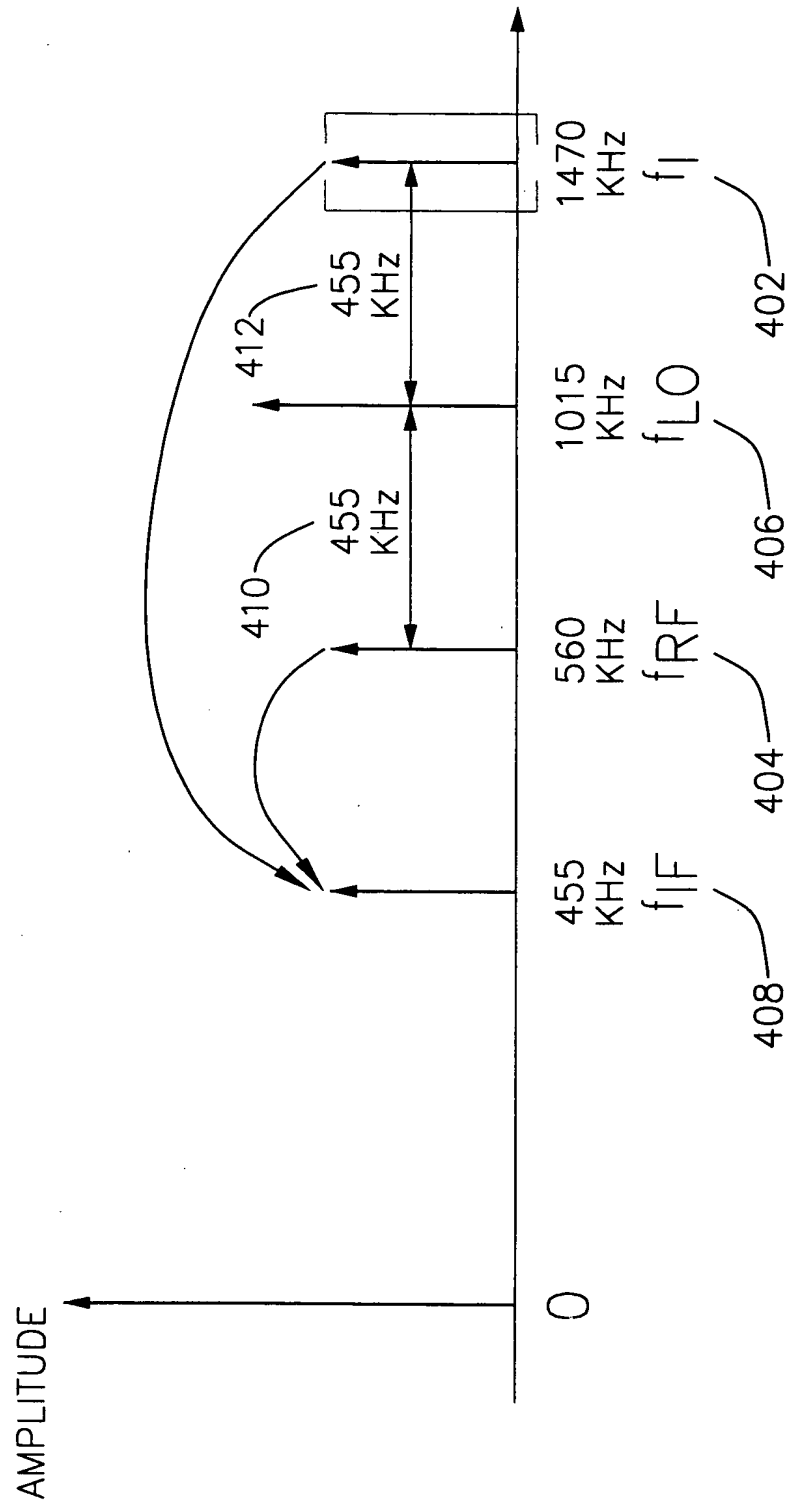


FIG.5
 DUAL CONVERSION RECEIVER

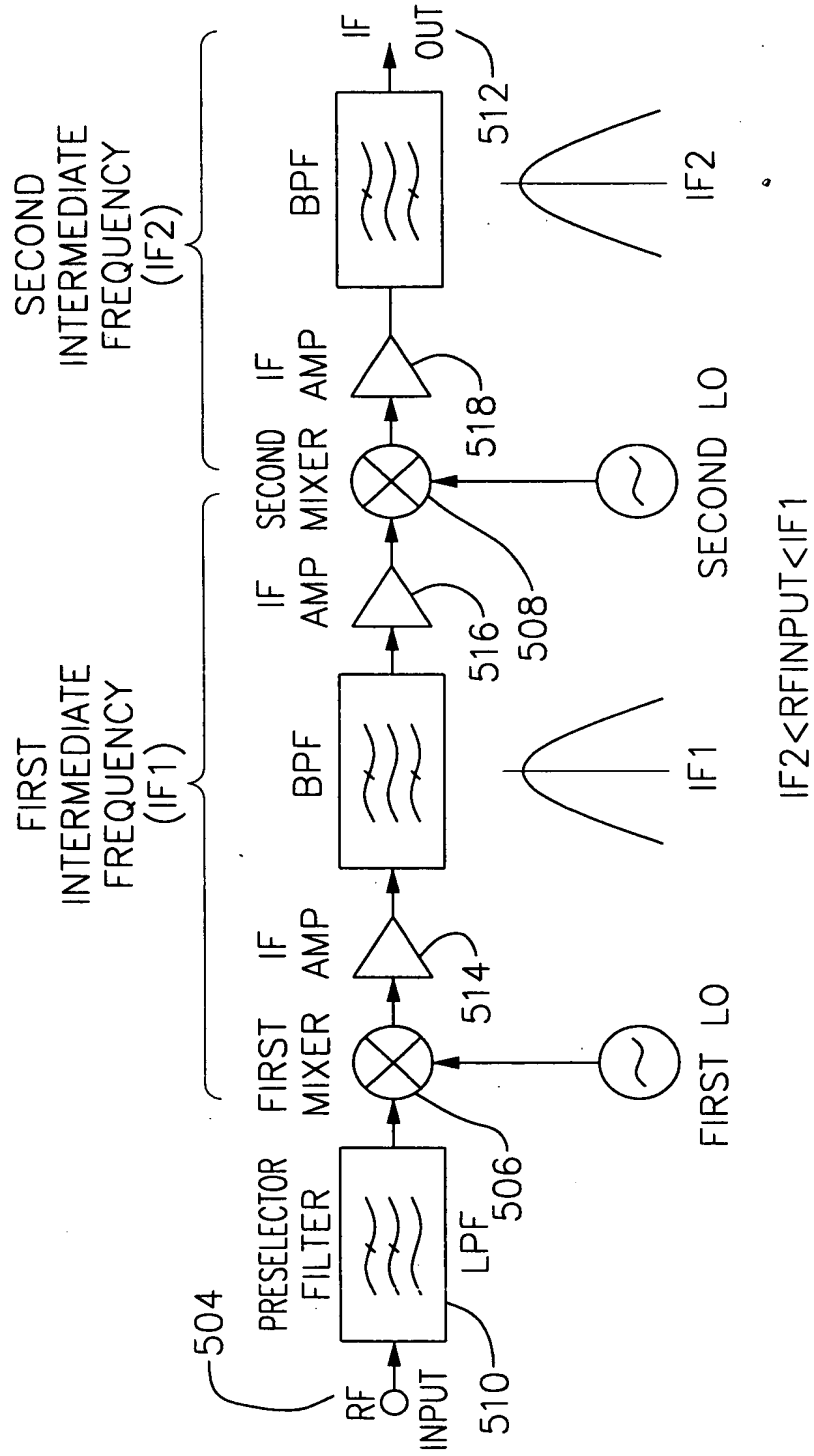


FIG. 6

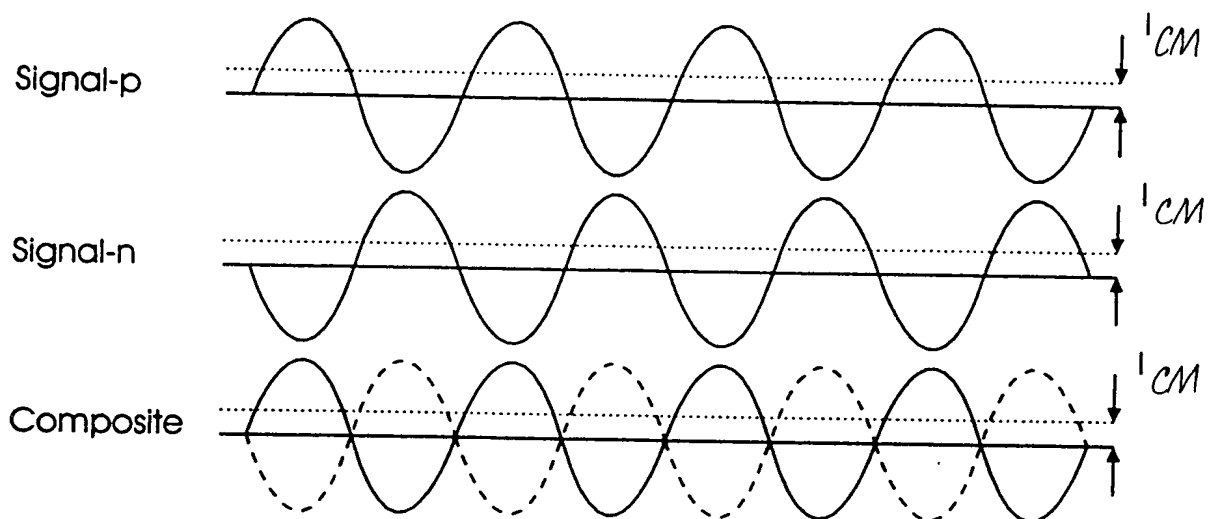


FIG. 7

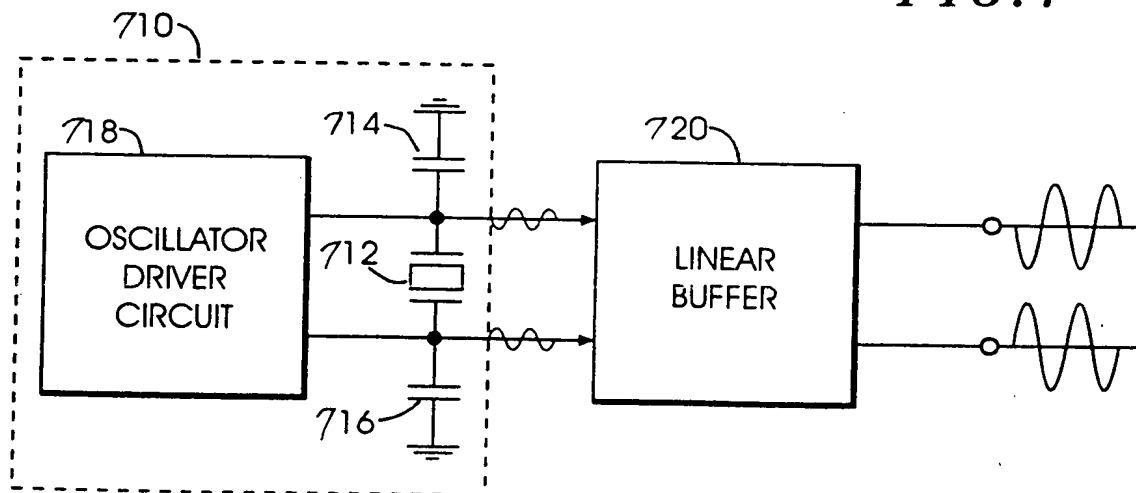


FIG. 8

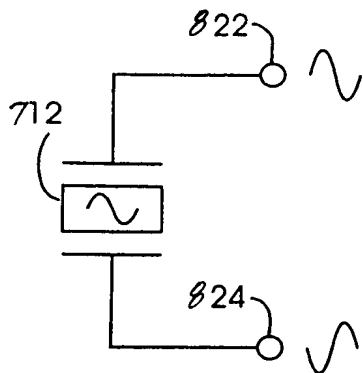


FIG. 9

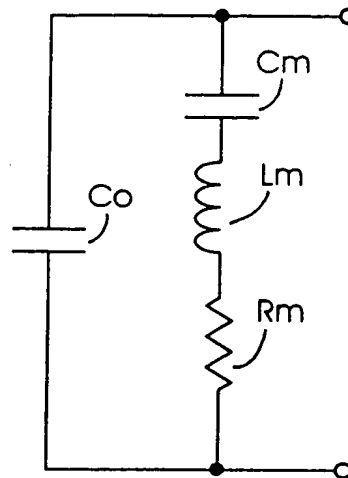


FIG. 10

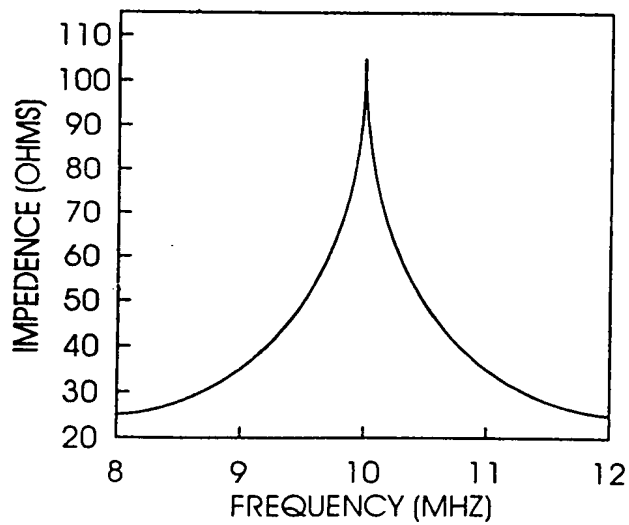
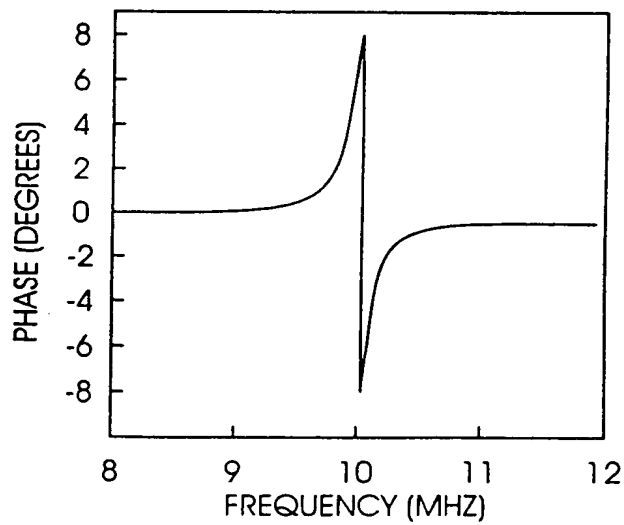


FIG. 11



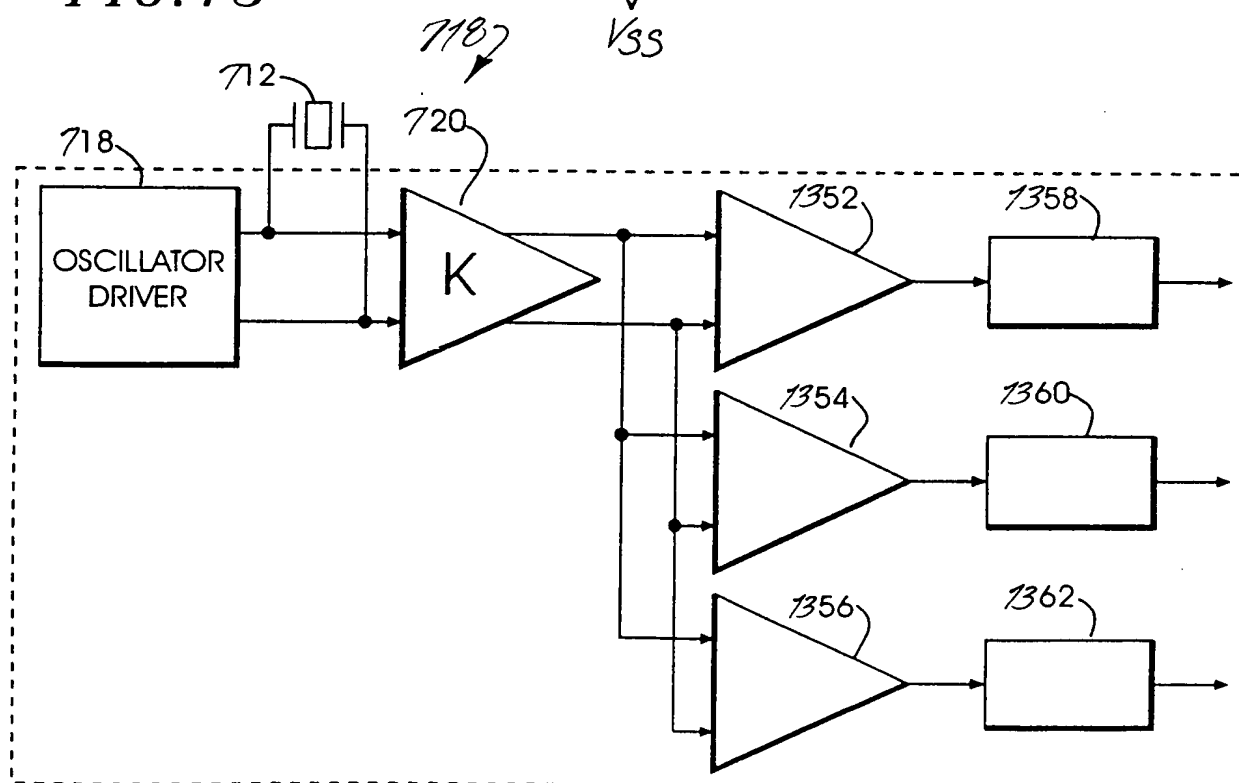
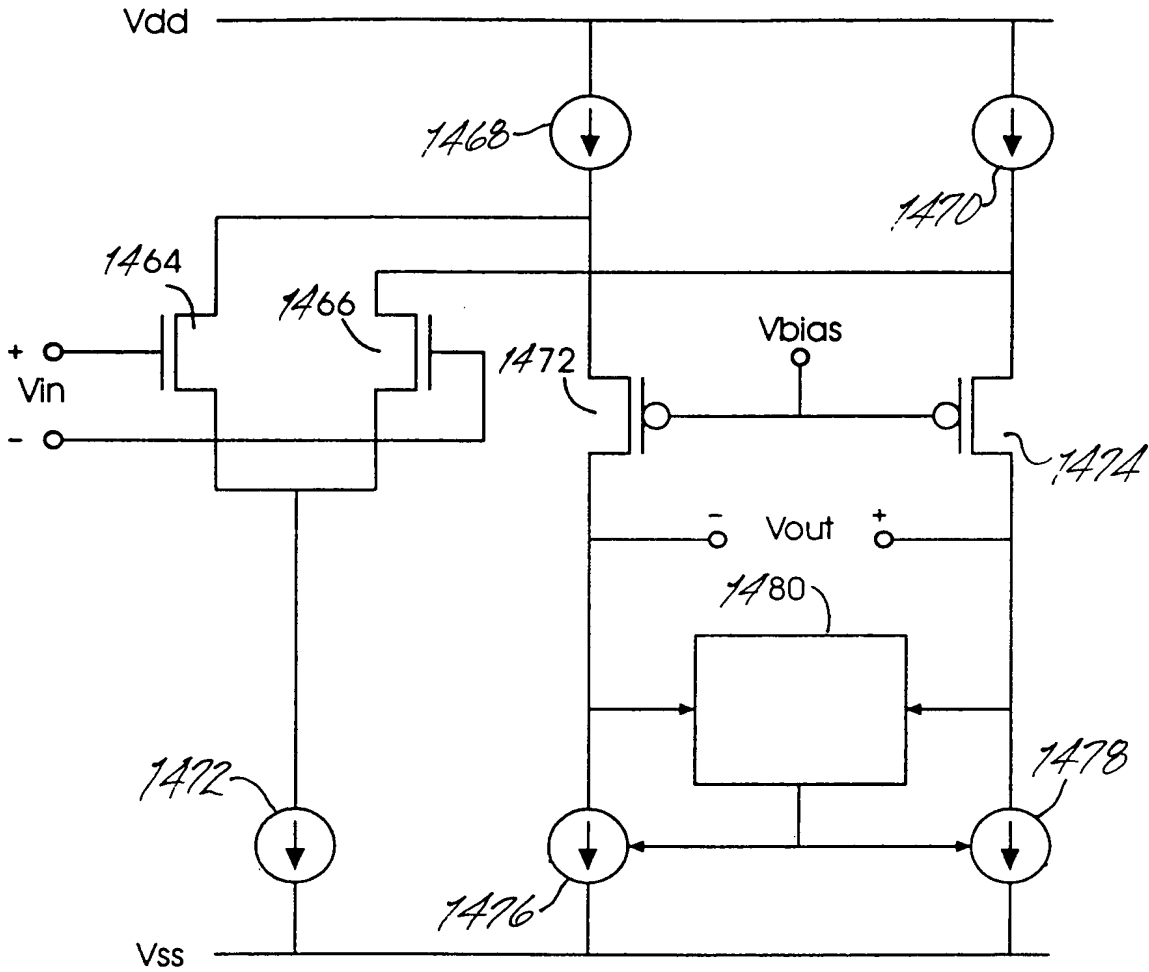


FIG. 14



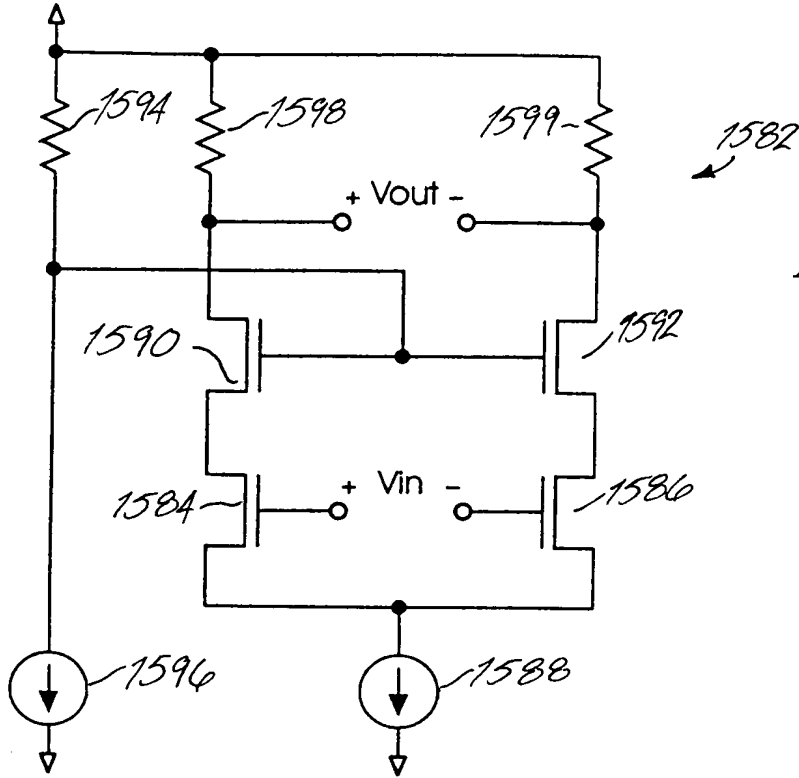


FIG. 15

FIG. 16

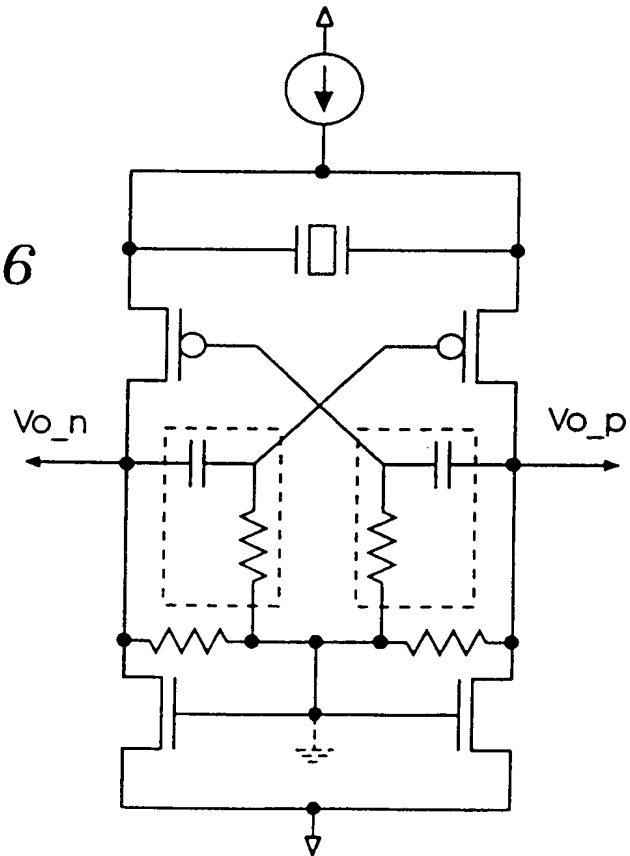


FIG. 17

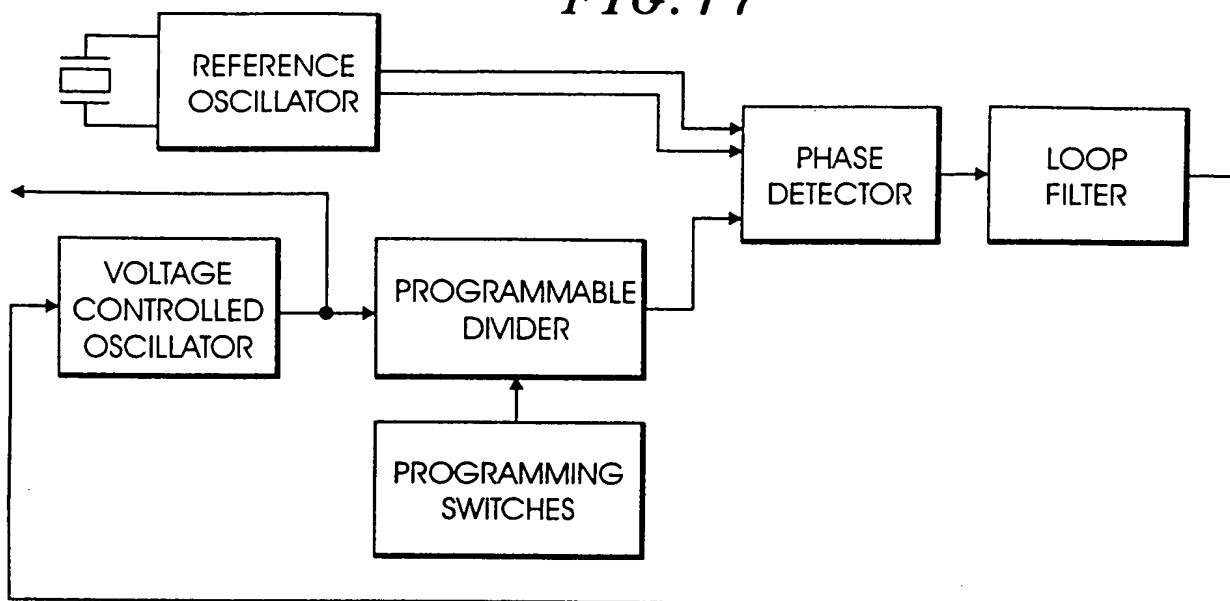


FIG. 18

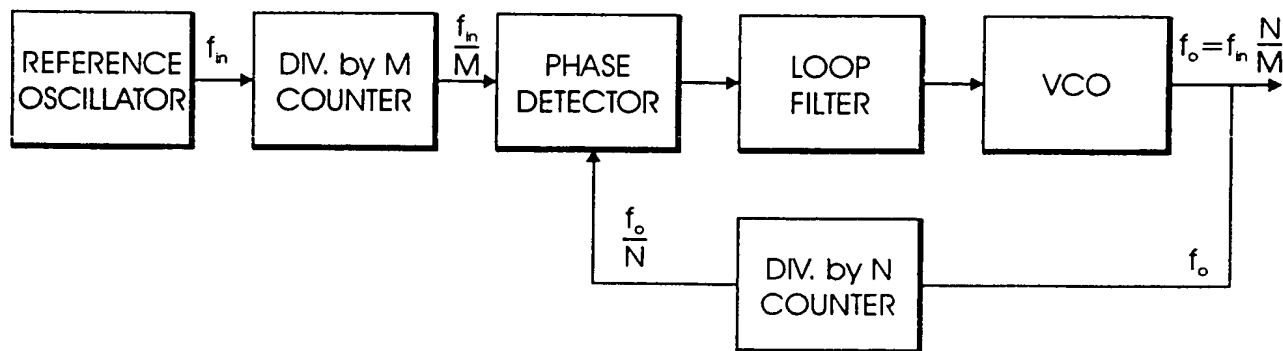


FIG. 19

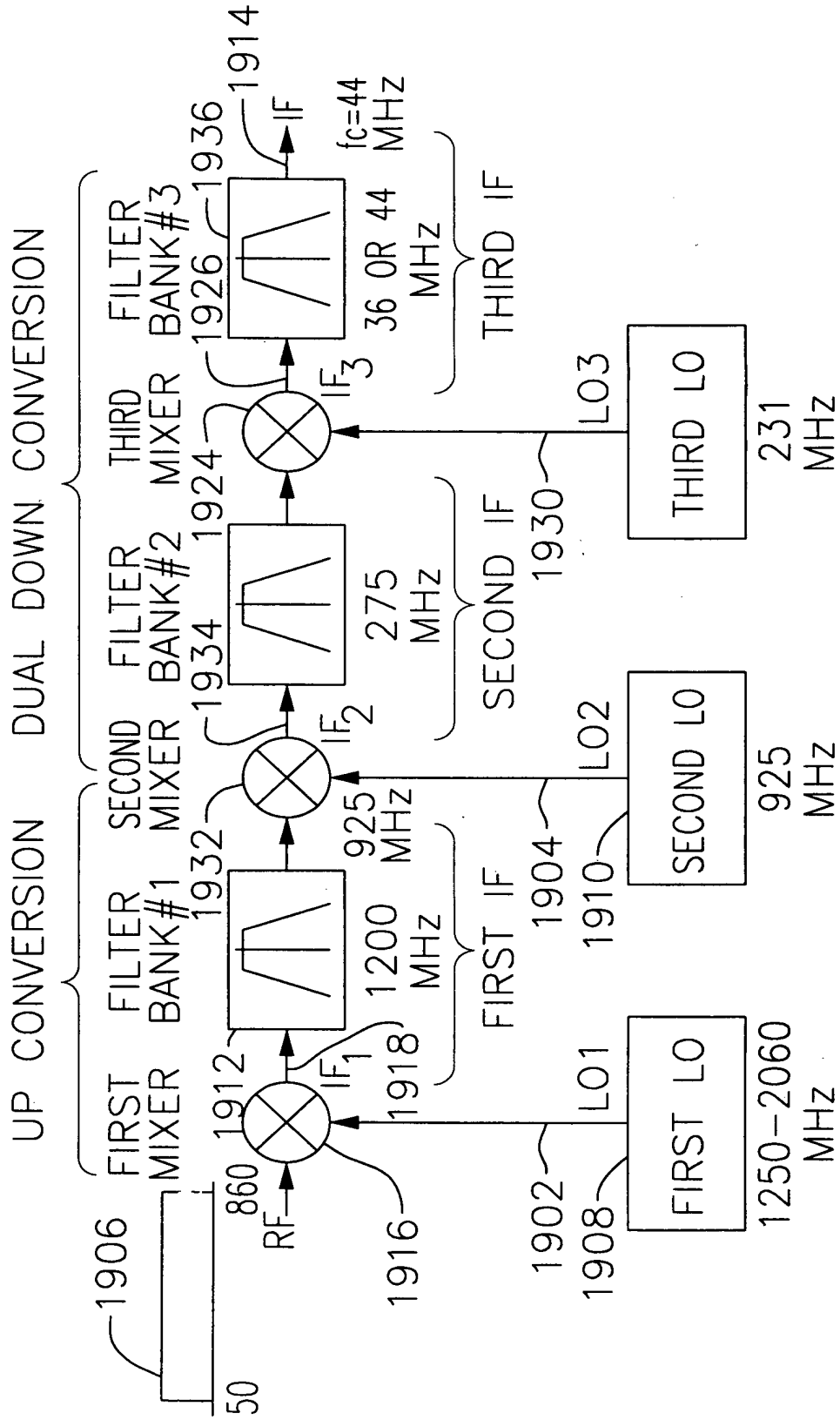


FIG. 20

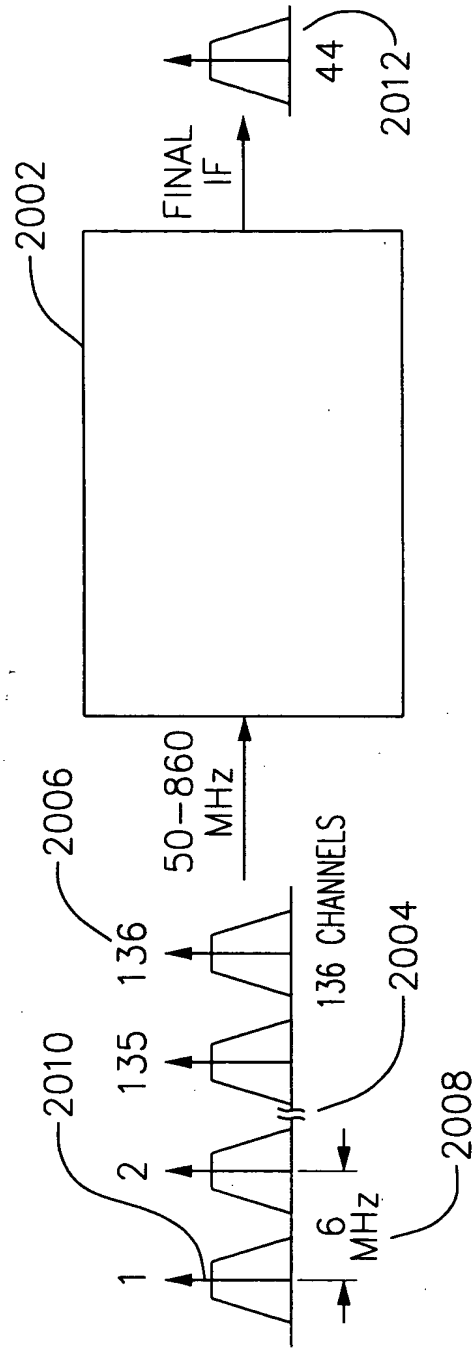


FIG. 21

PPL Xtal REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

44MHz IF

NOTE
 •LO-2 REF=100KHz,
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Frq (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2(MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2(MHz)	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102

FIG.22

PPL Xtol REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

36MHz IF

NOTE
•LO-2 REF=100KHz,
SO DIVIDE RANGE=9280 TO 9340

TABLE OF FREQUENCIES BASED ON
COARSE/FINE PLL SOLUTION:

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG. 23

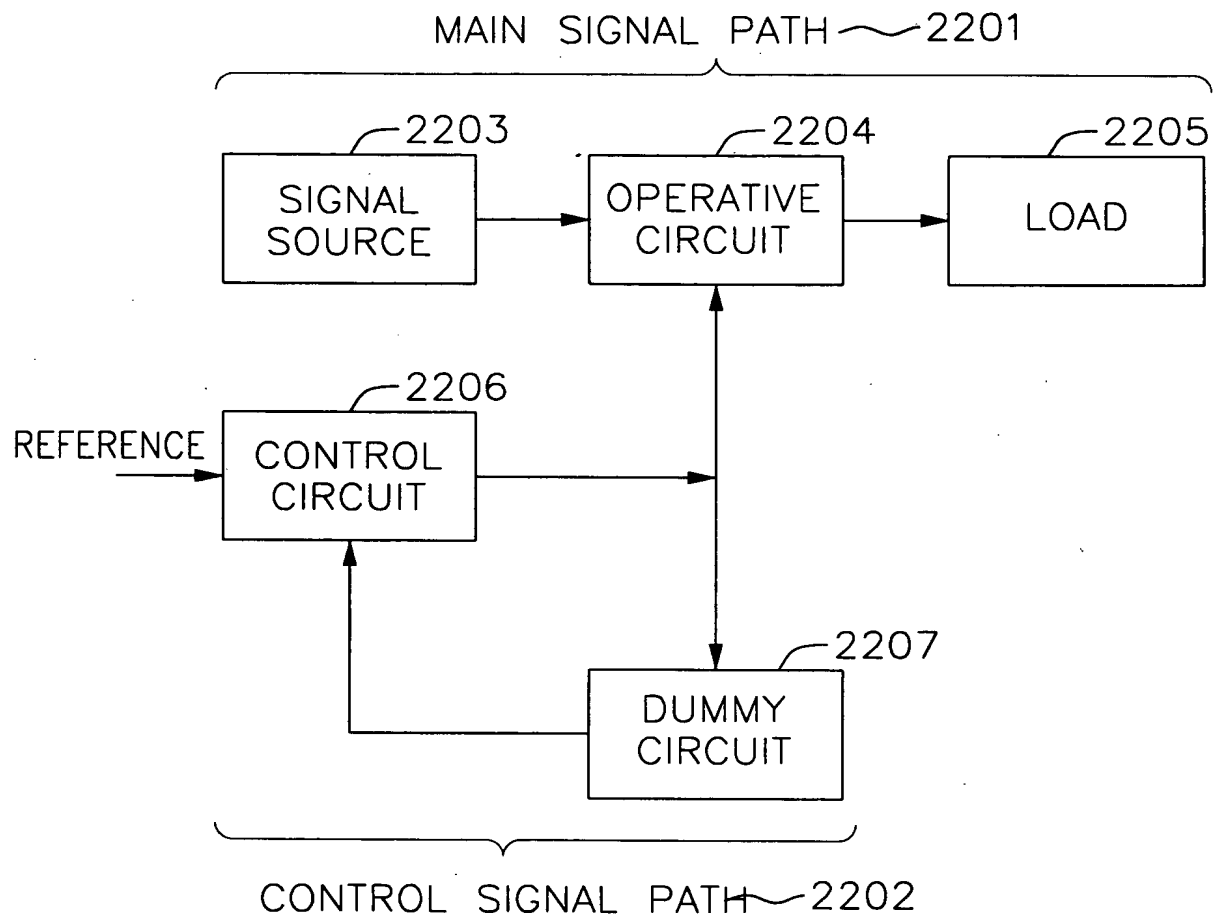


FIG. 24a

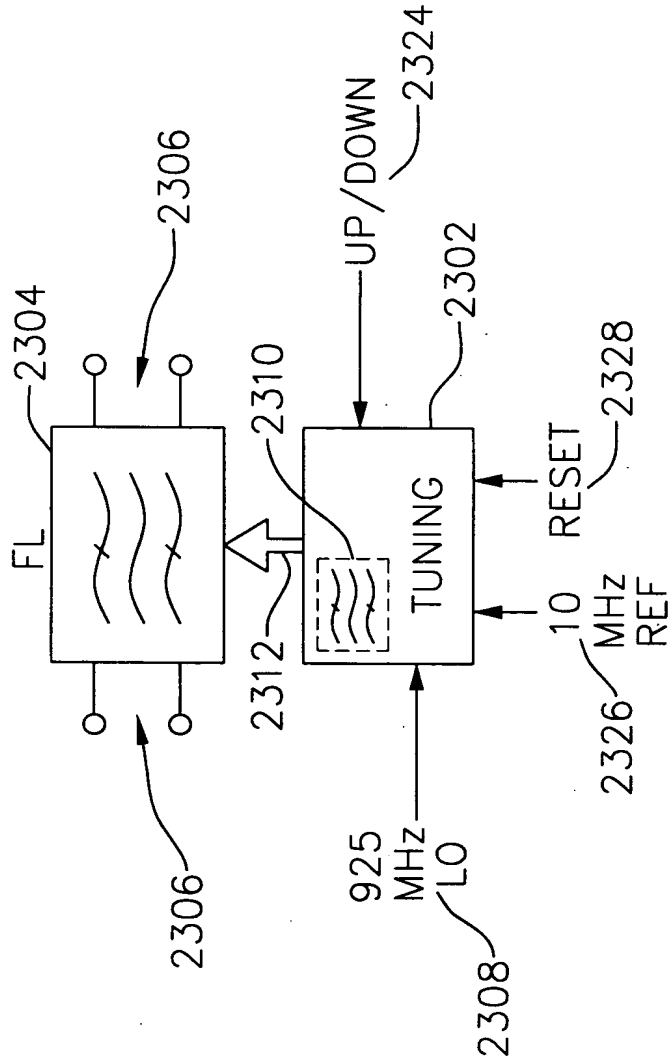


FIG. 24b

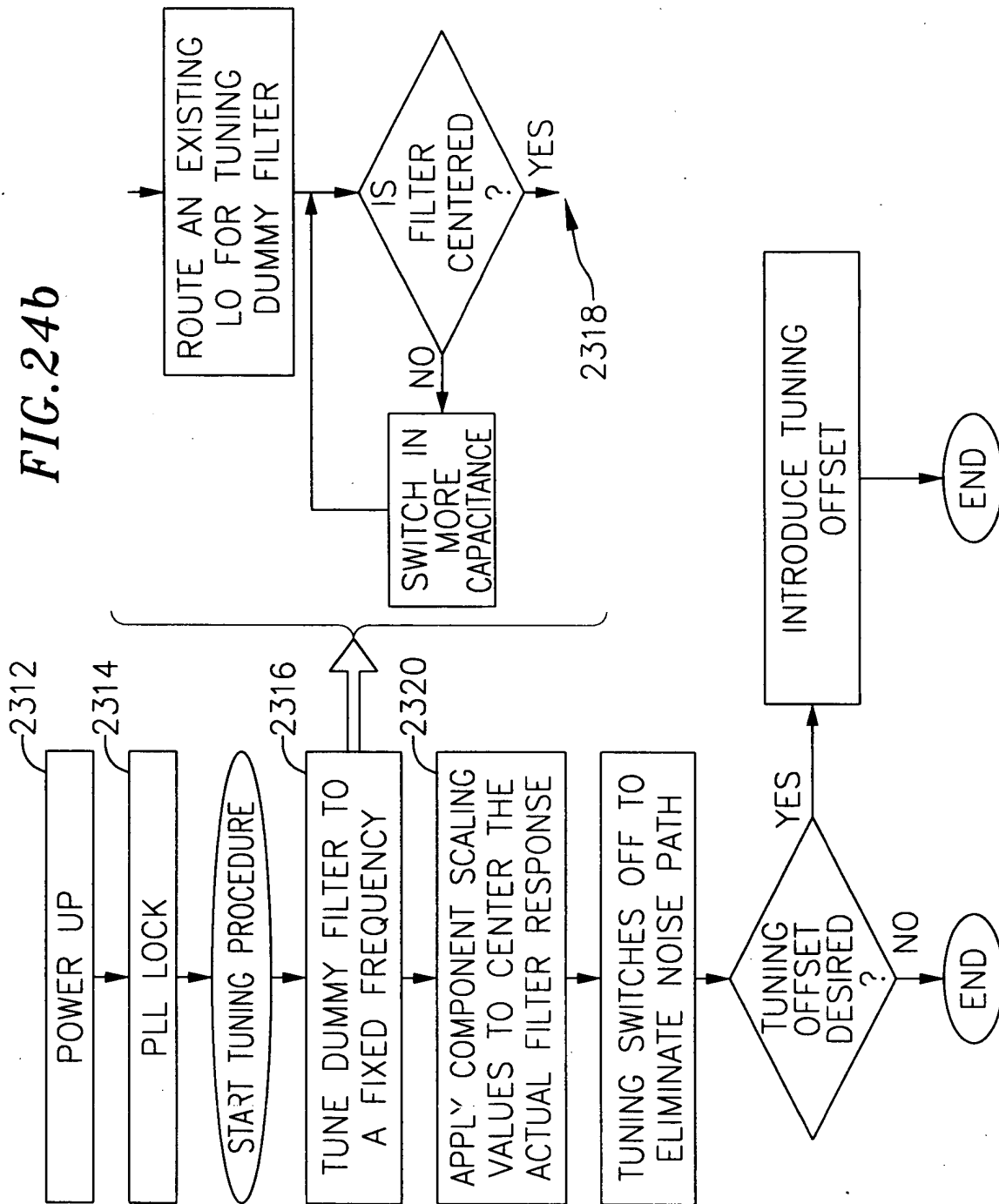


FIG. 24c

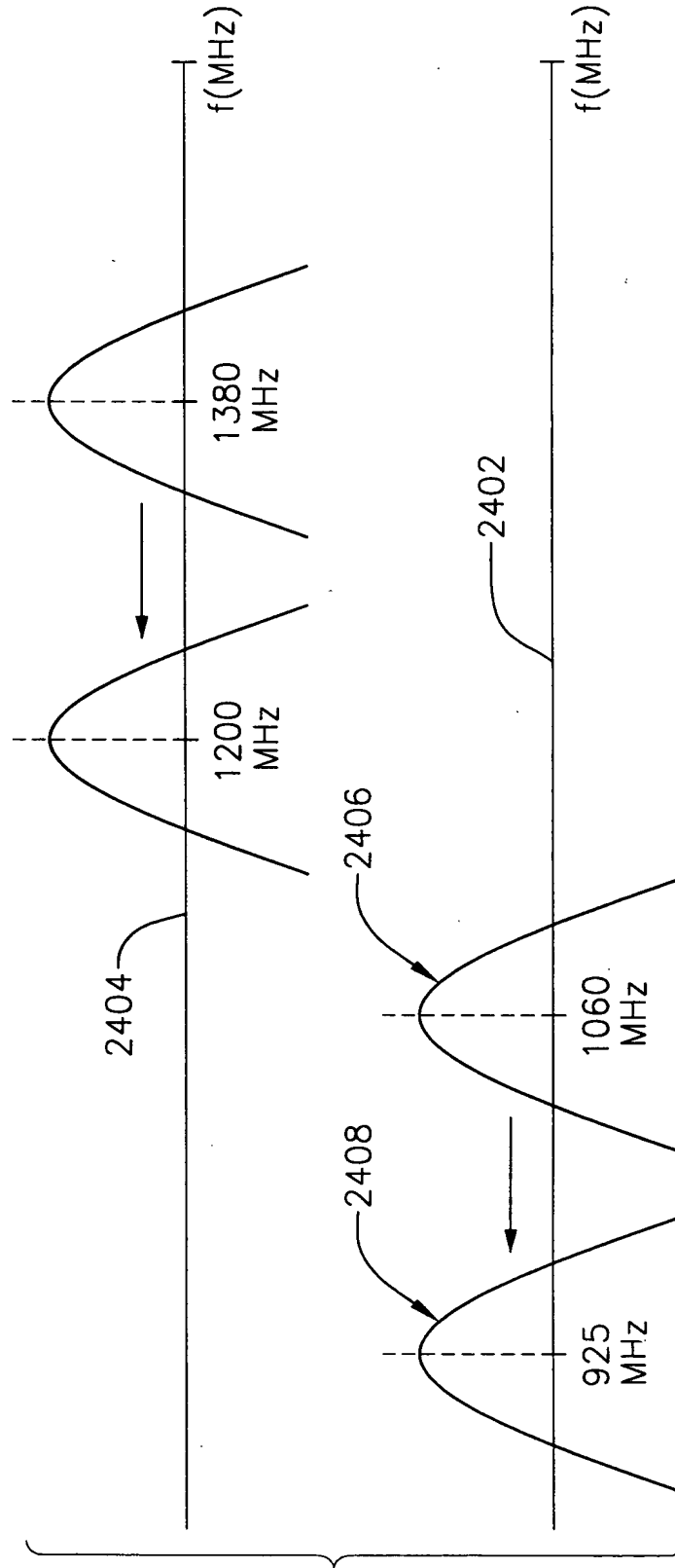


FIG. 25

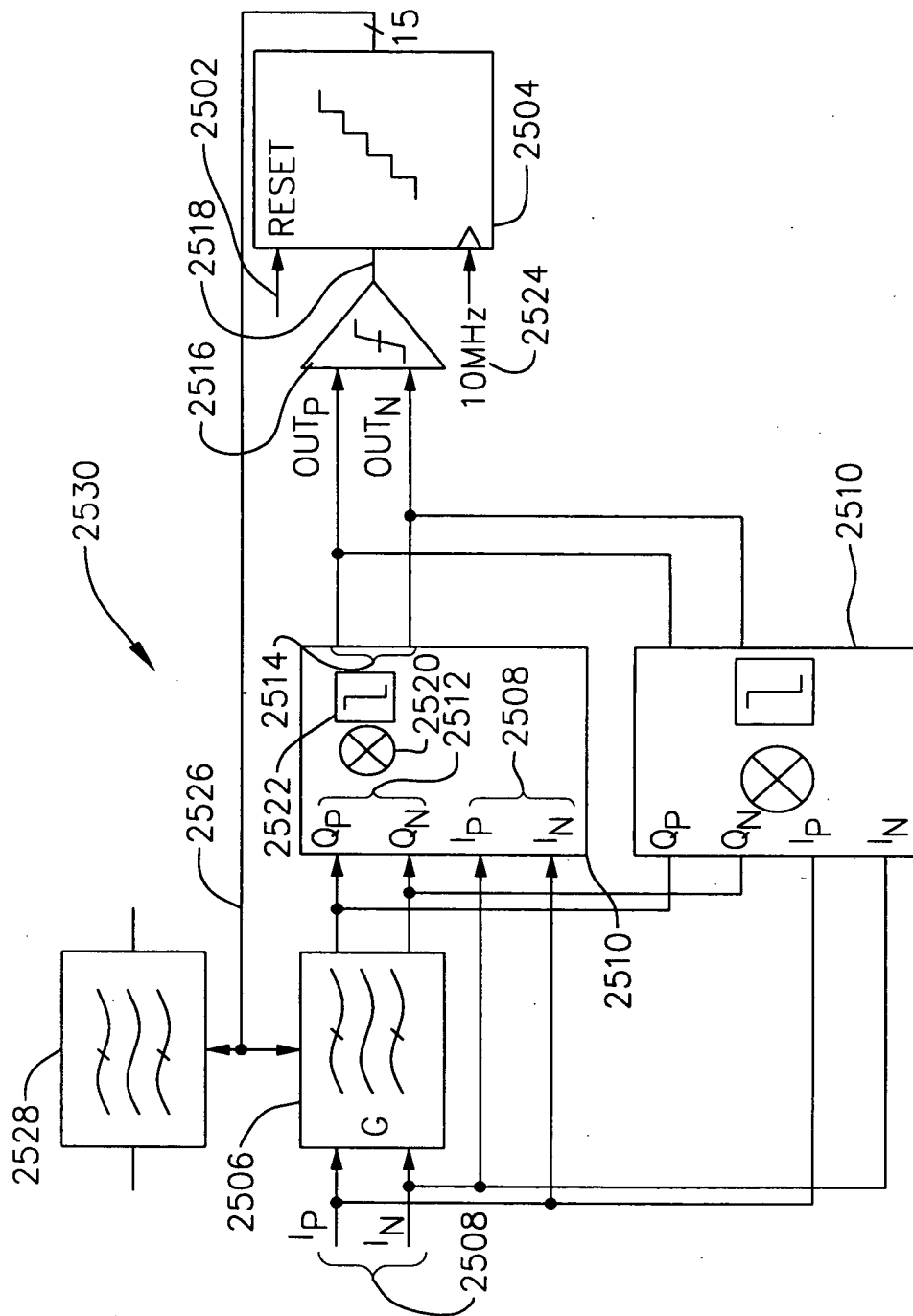
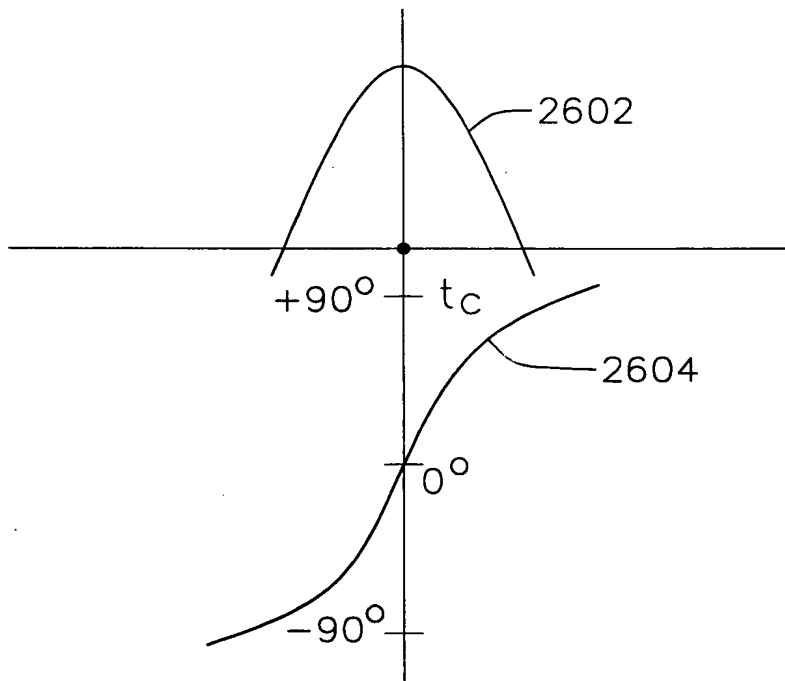


FIG. 26



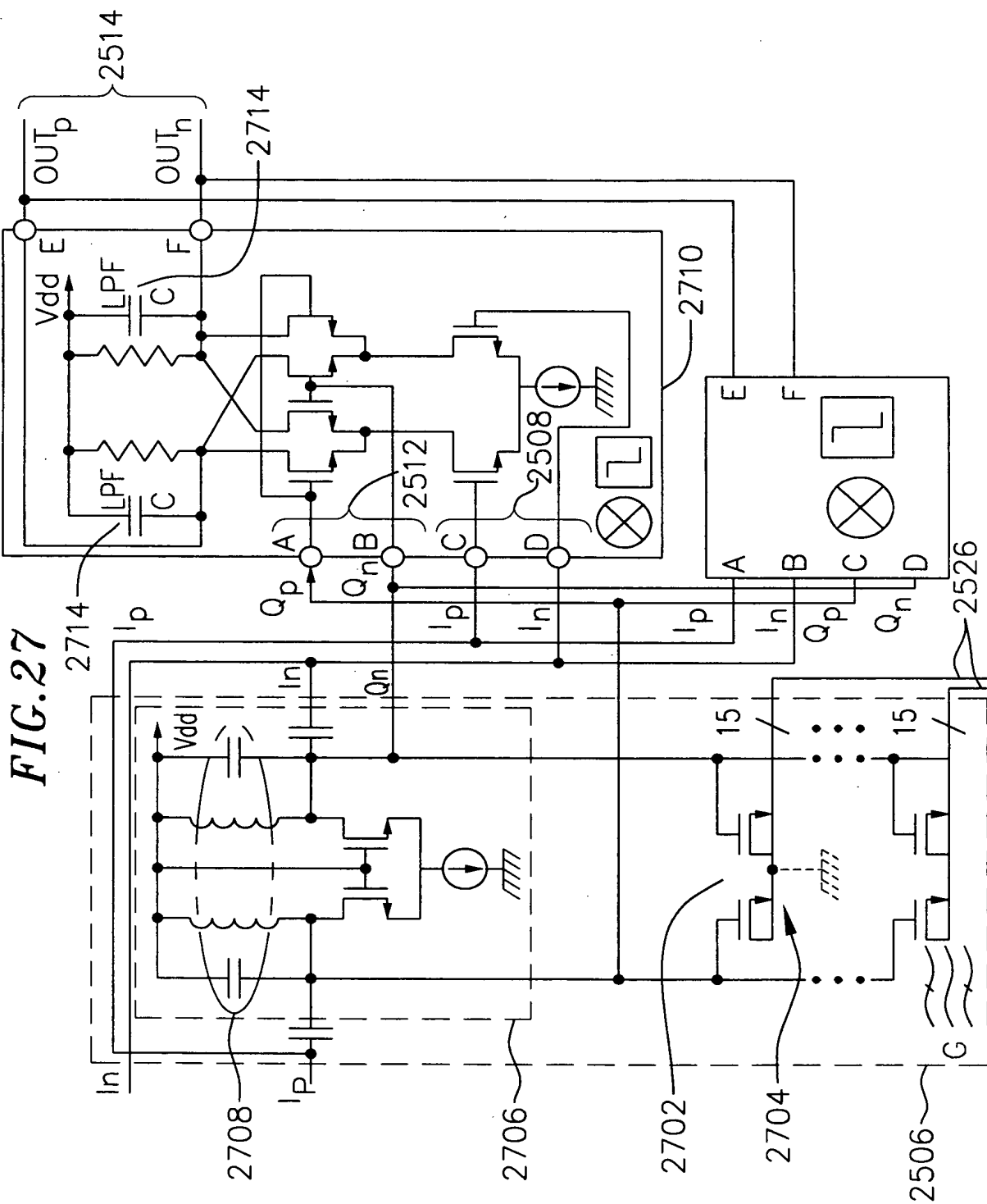


FIG.28

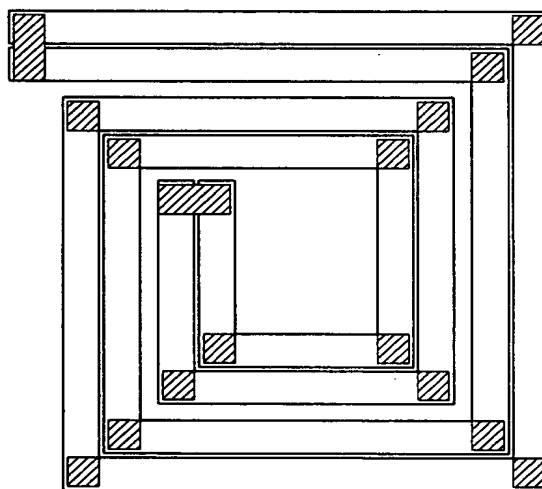


FIG. 29

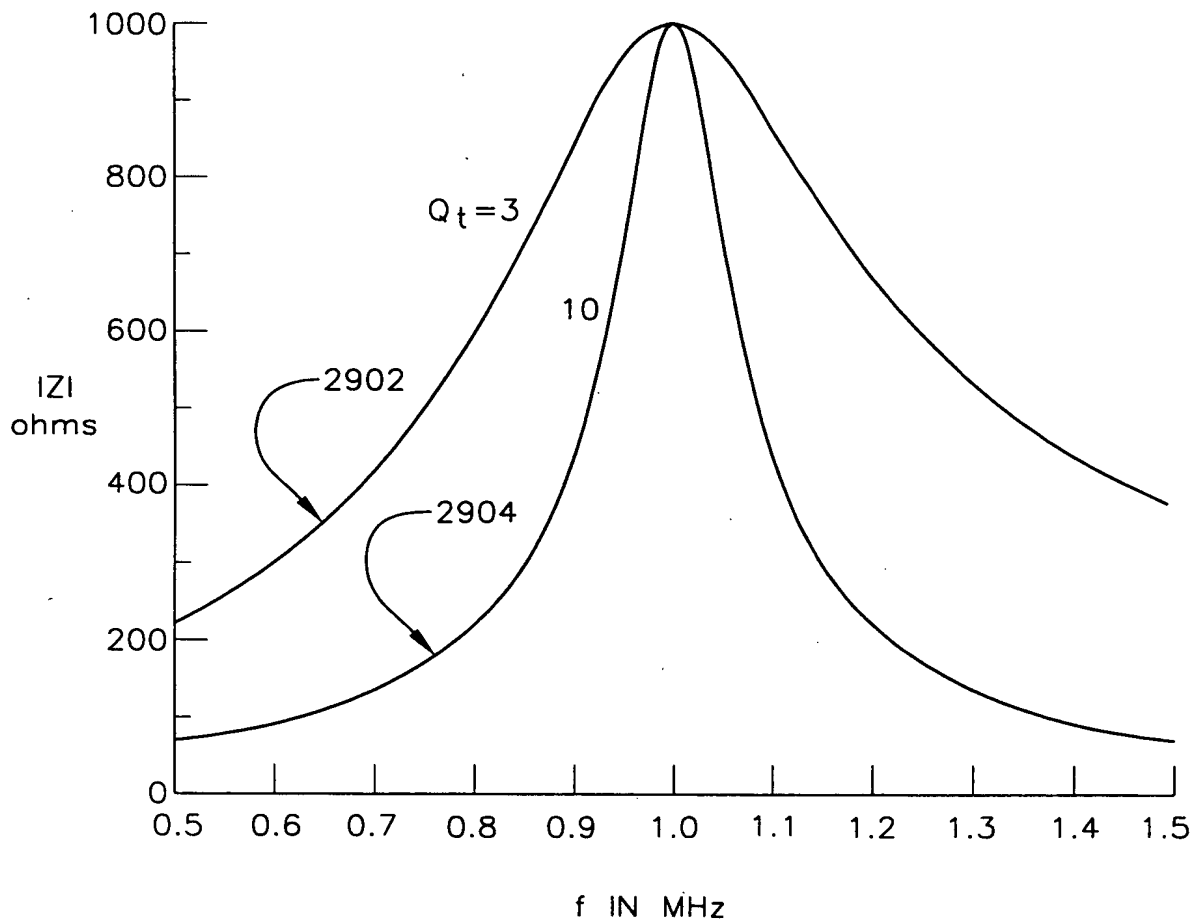


FIG. 30

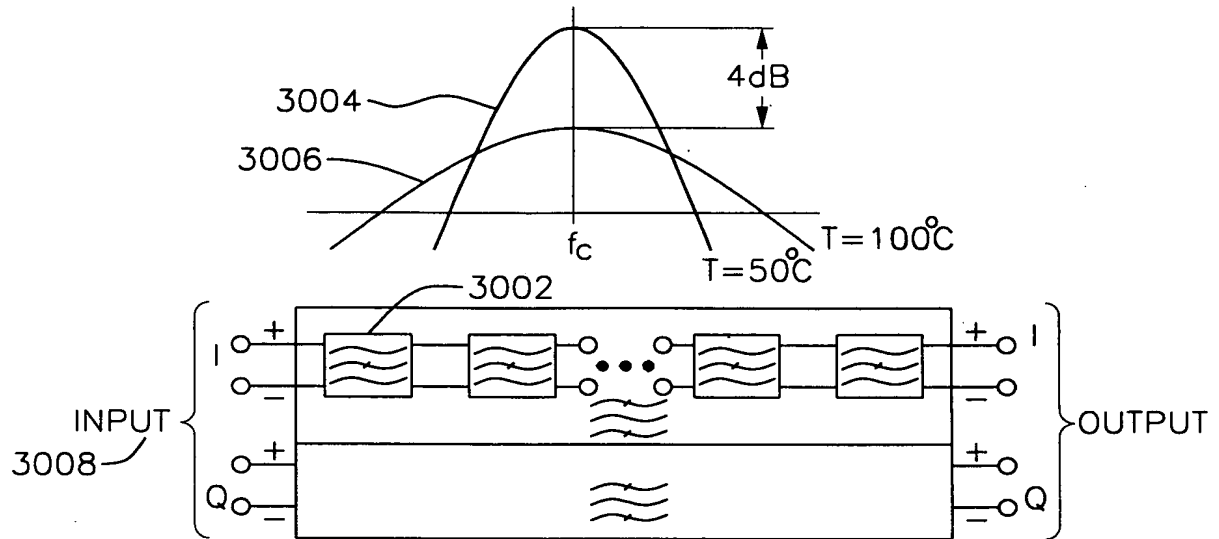


FIG. 31

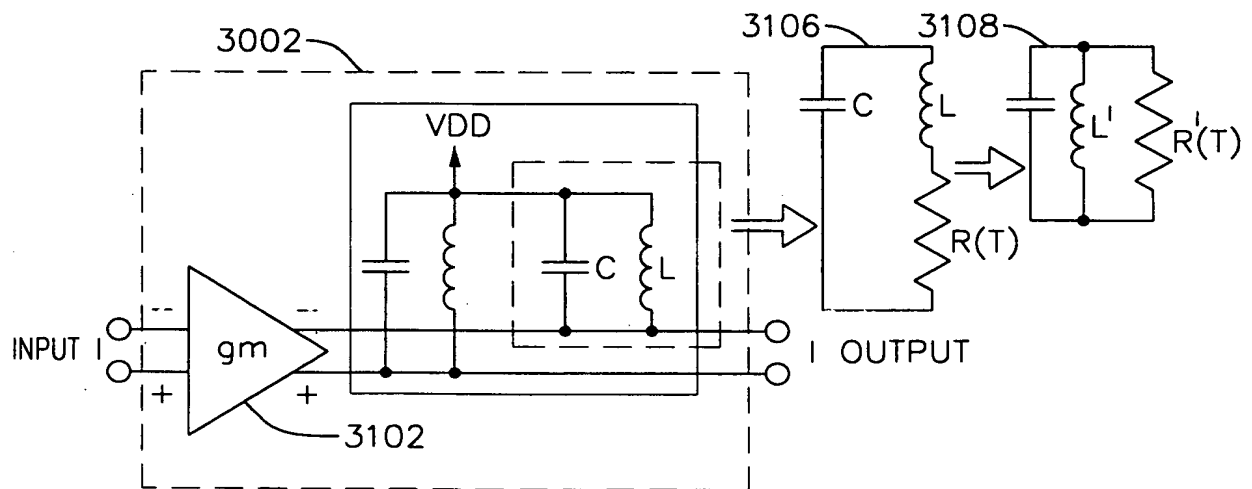


FIG. 32

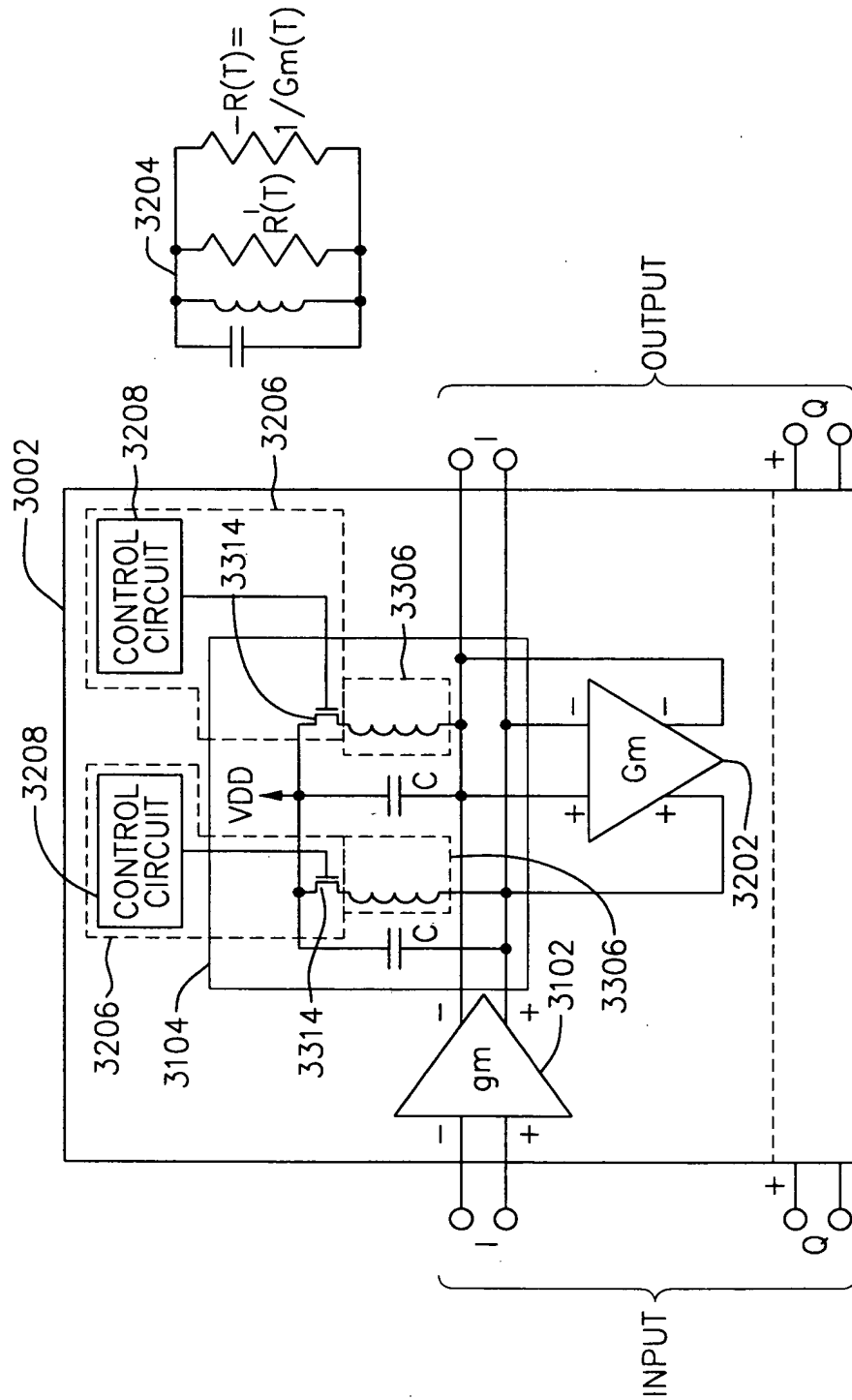


FIG. 33

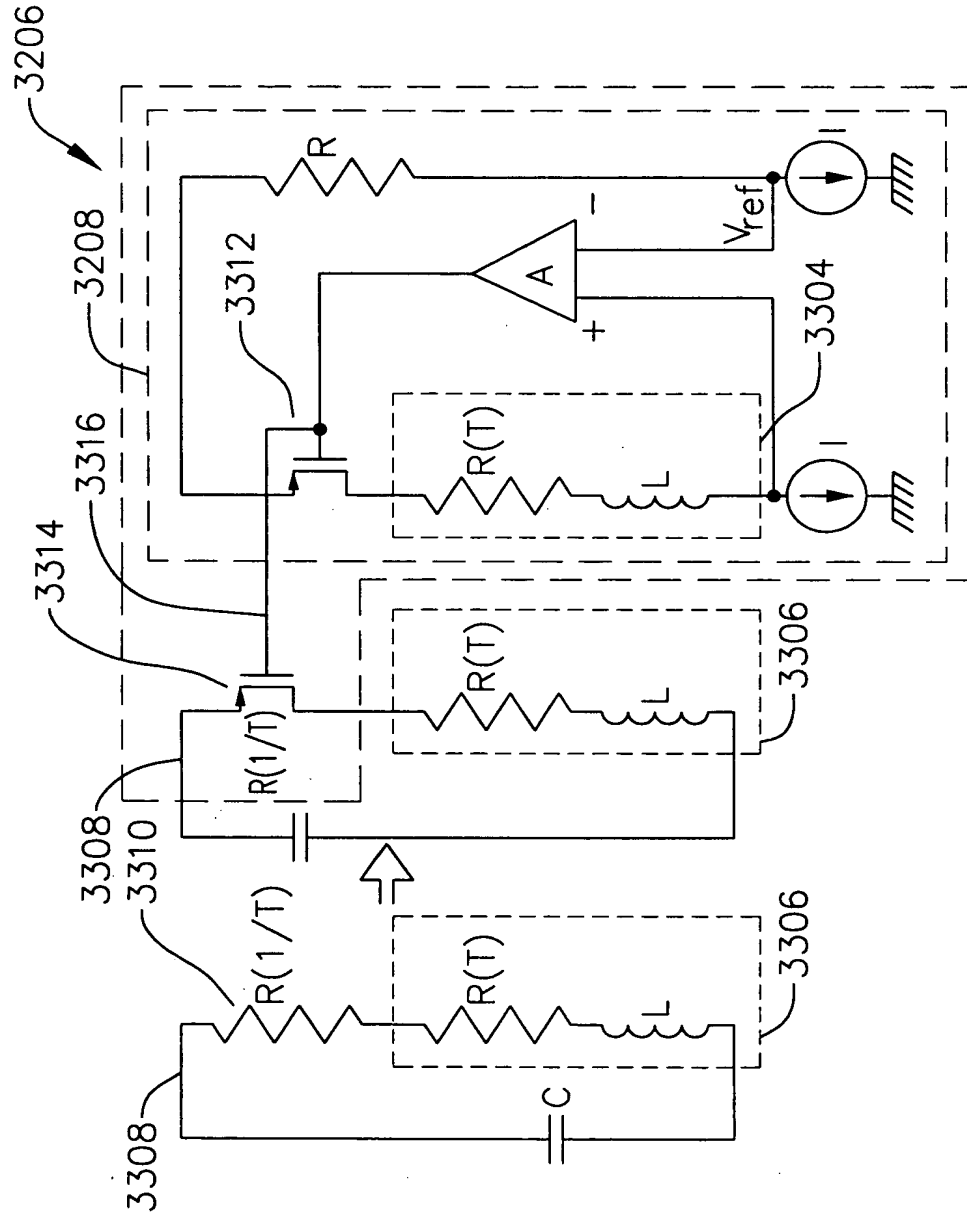


FIG. 34

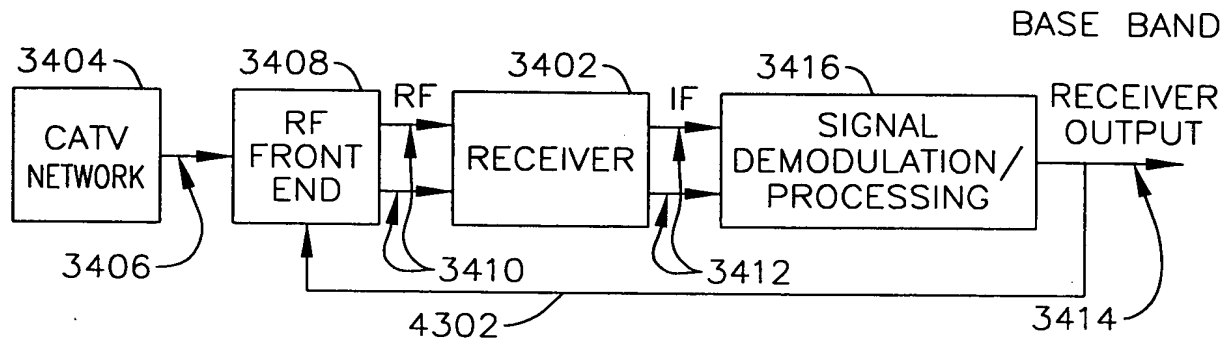
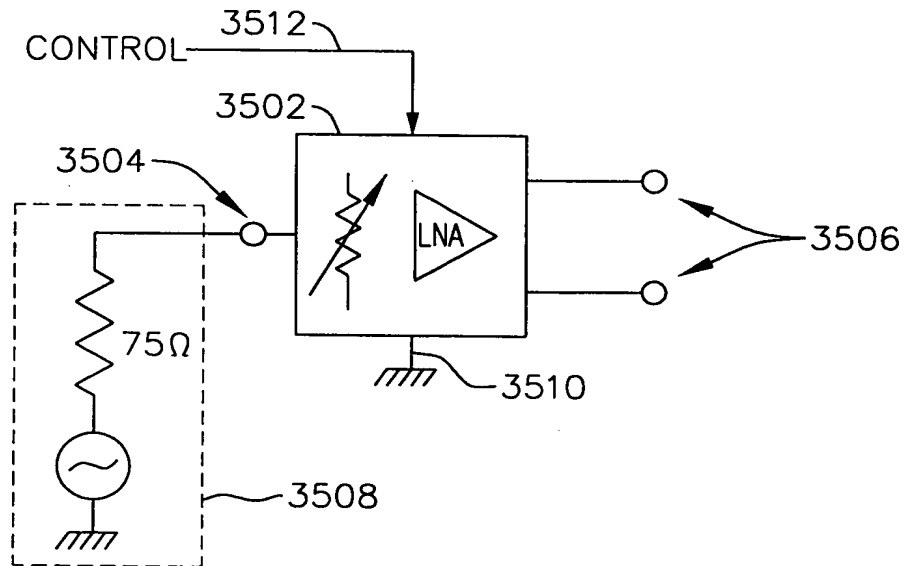


FIG. 35



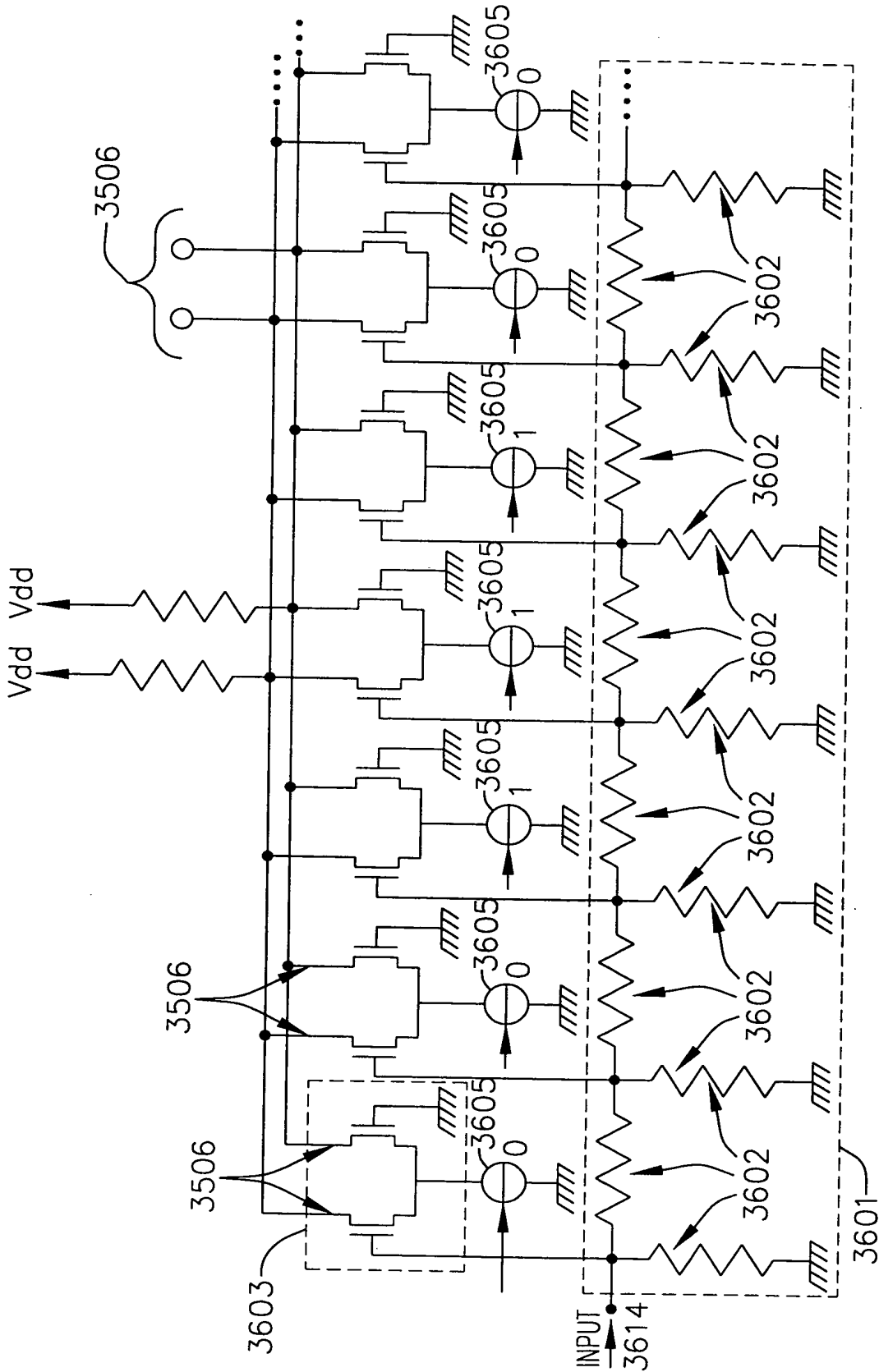
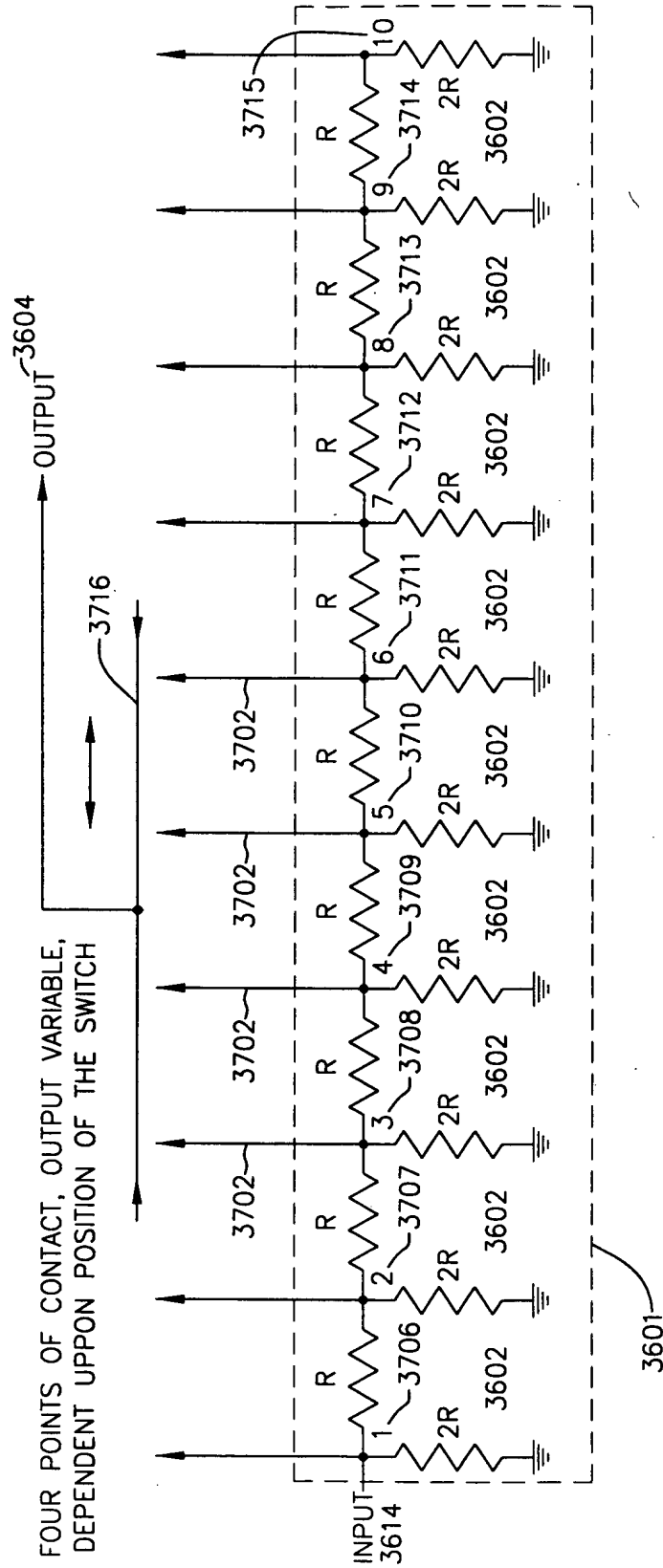


FIG. 37



PGA SETTINGS

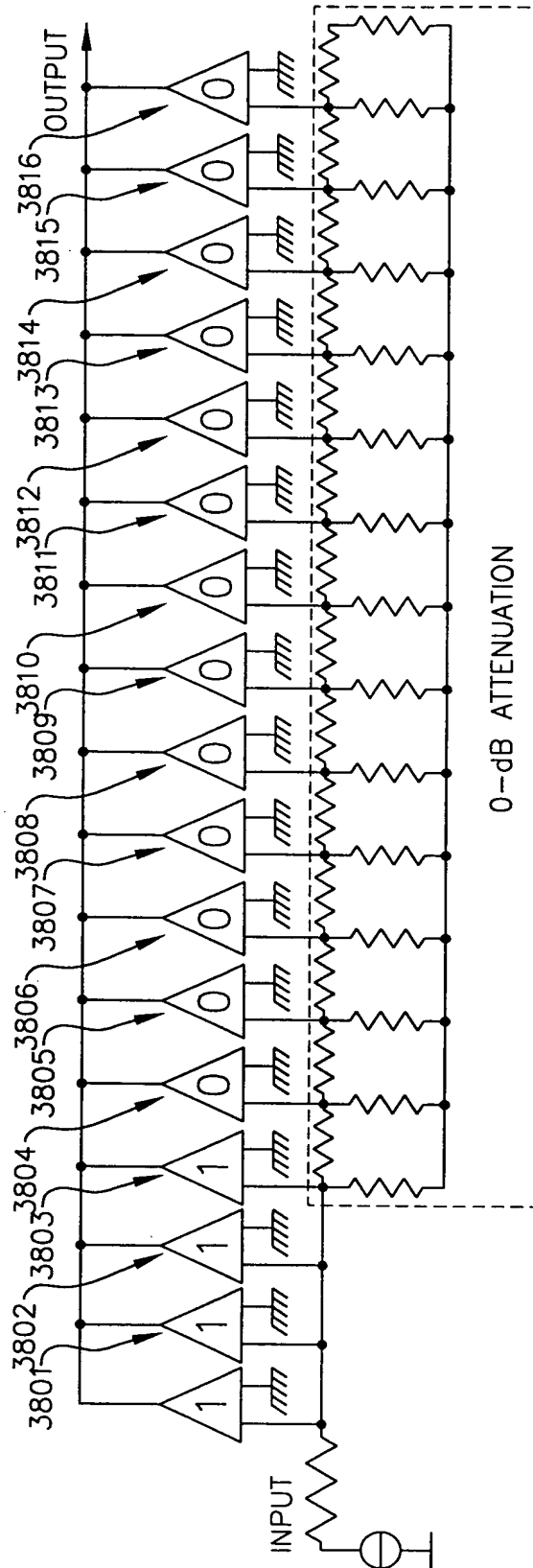


FIG. 39

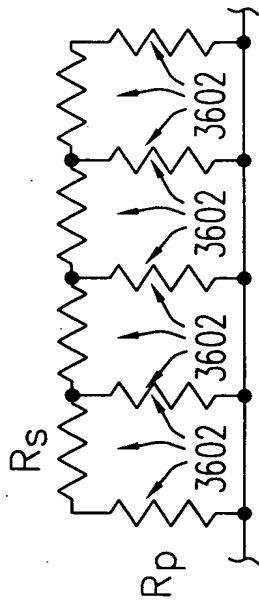


FIG. 40

PGA ARCHITECTURE

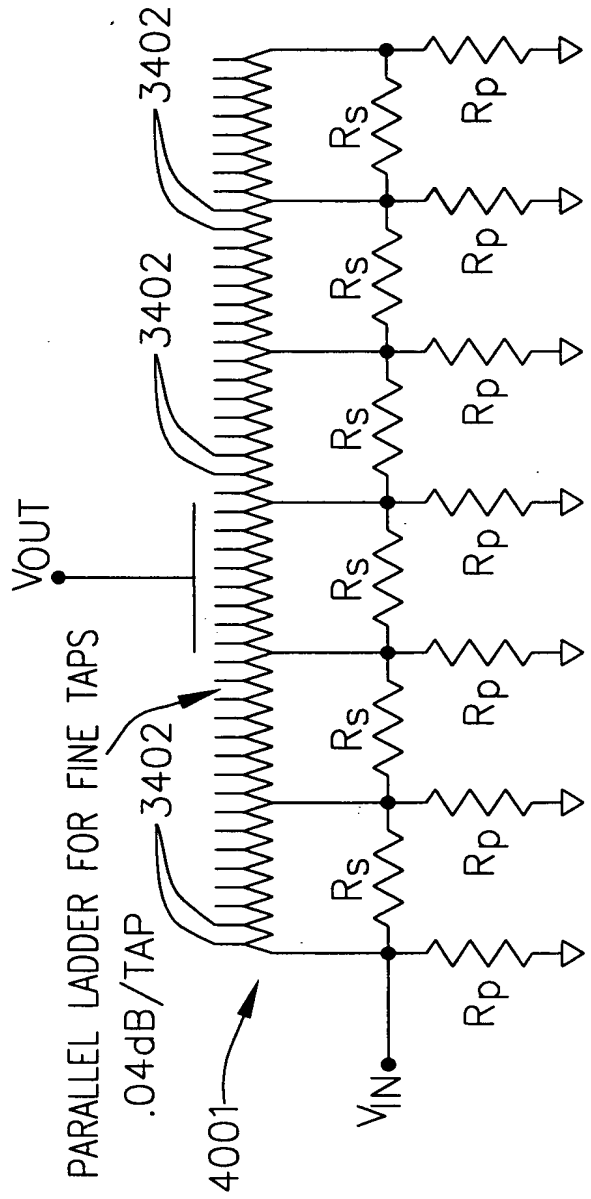


FIG. 41

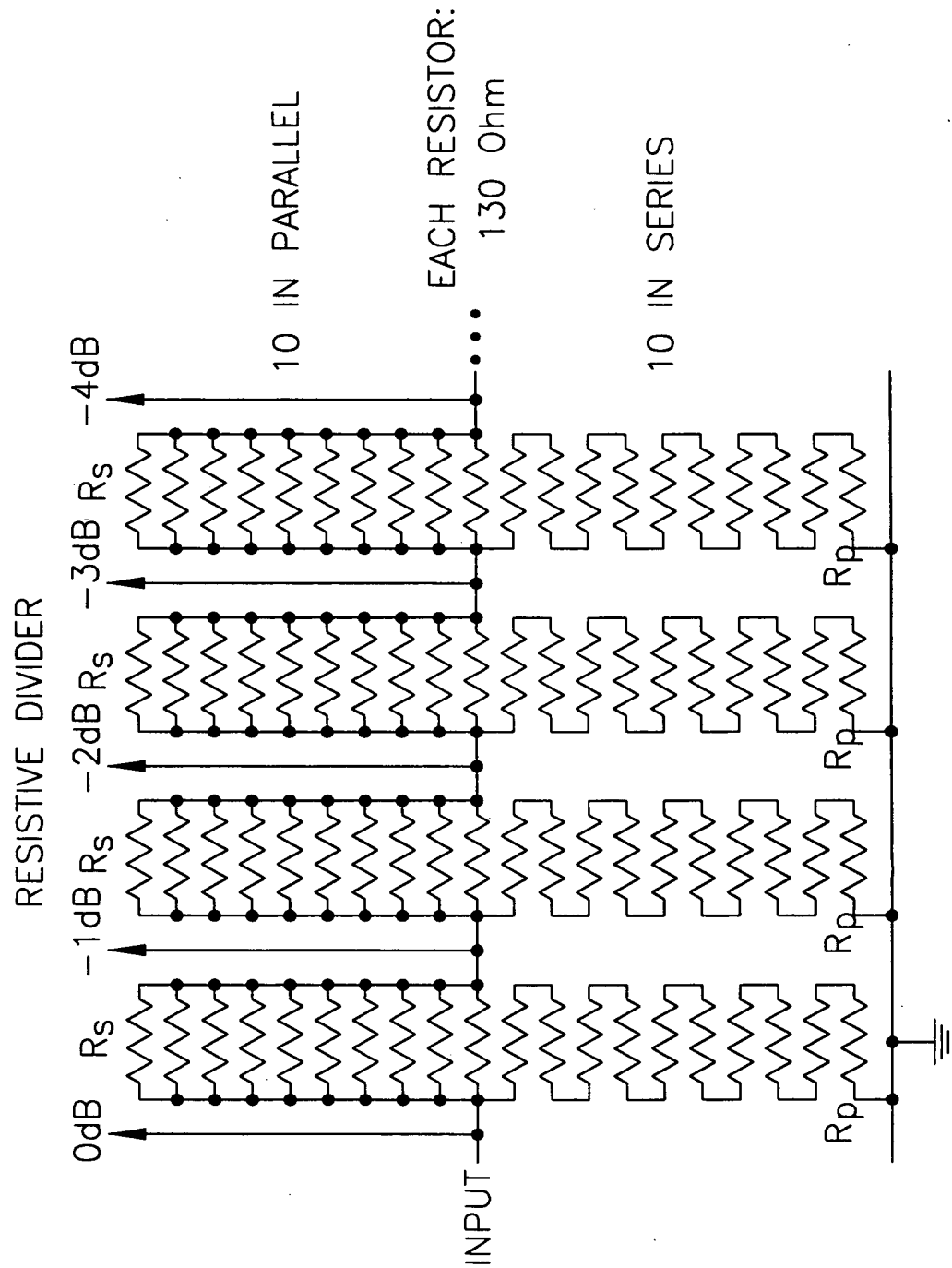


FIG. 42

NON-MONOTONICITY

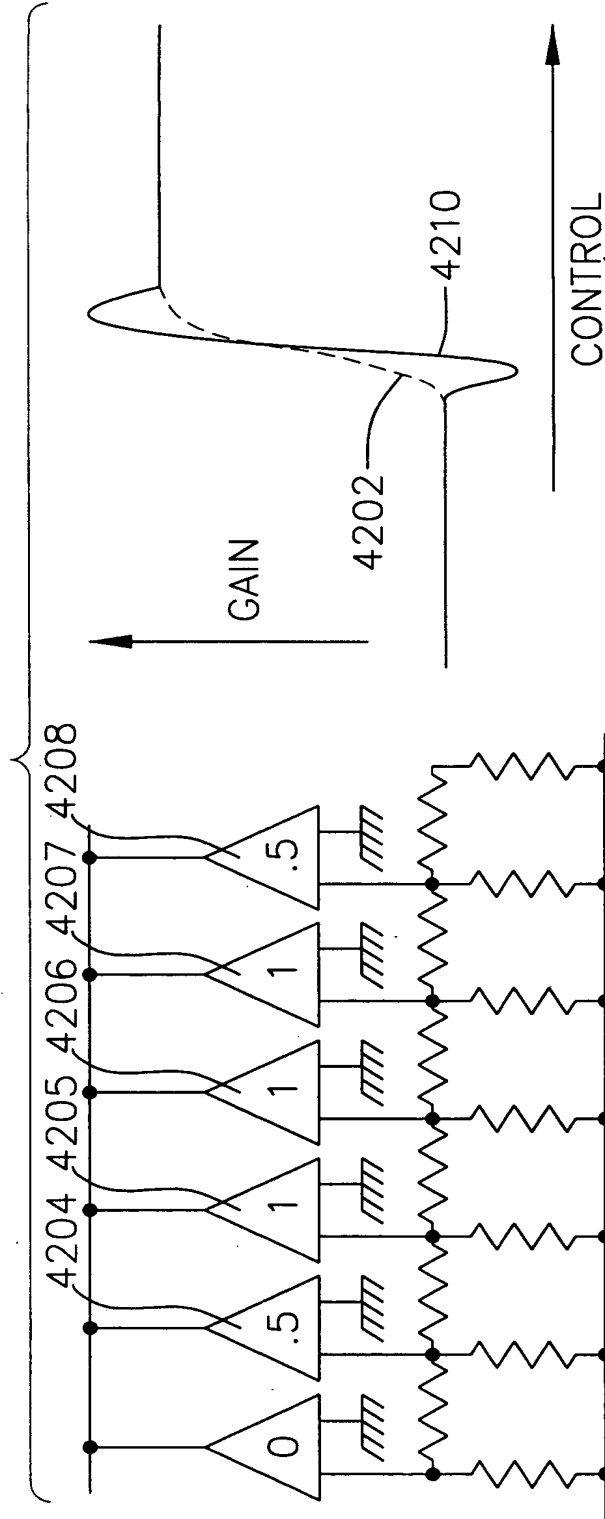


FIG. 43
 CLAMPING CONTROL RANGE

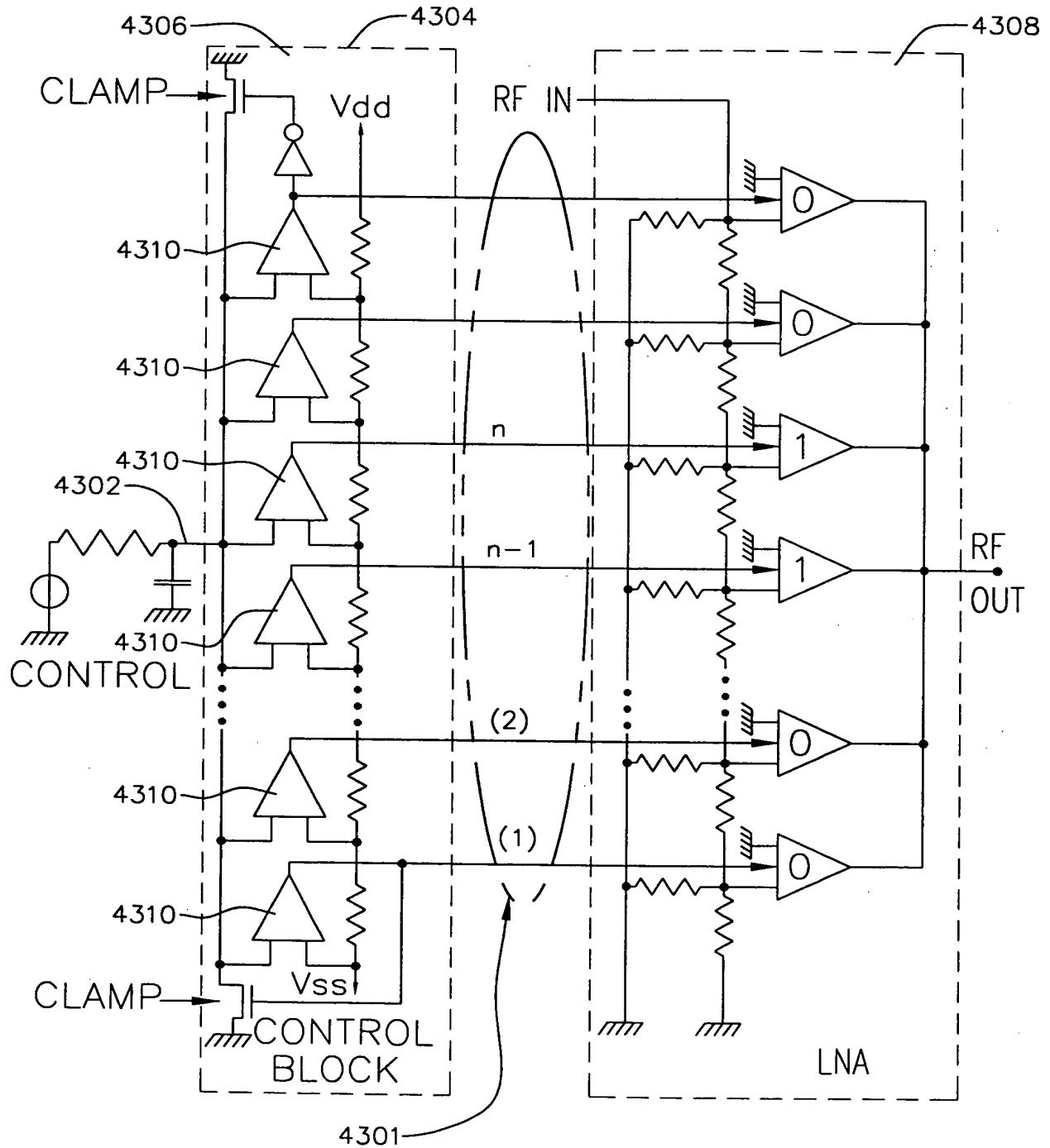


FIG. 44a
 CONTROLLED GAIN COMPARATOR

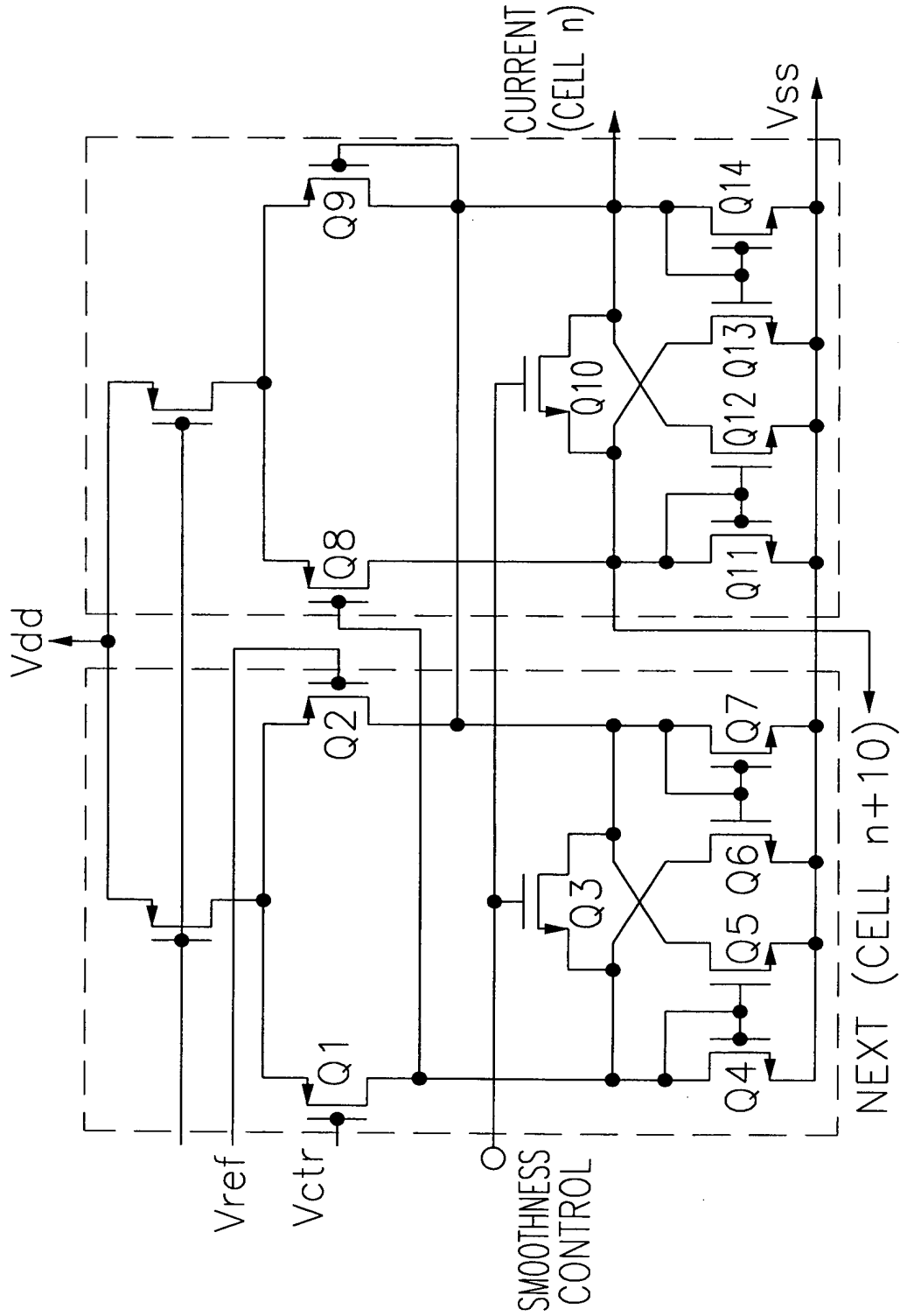


FIG. 44b

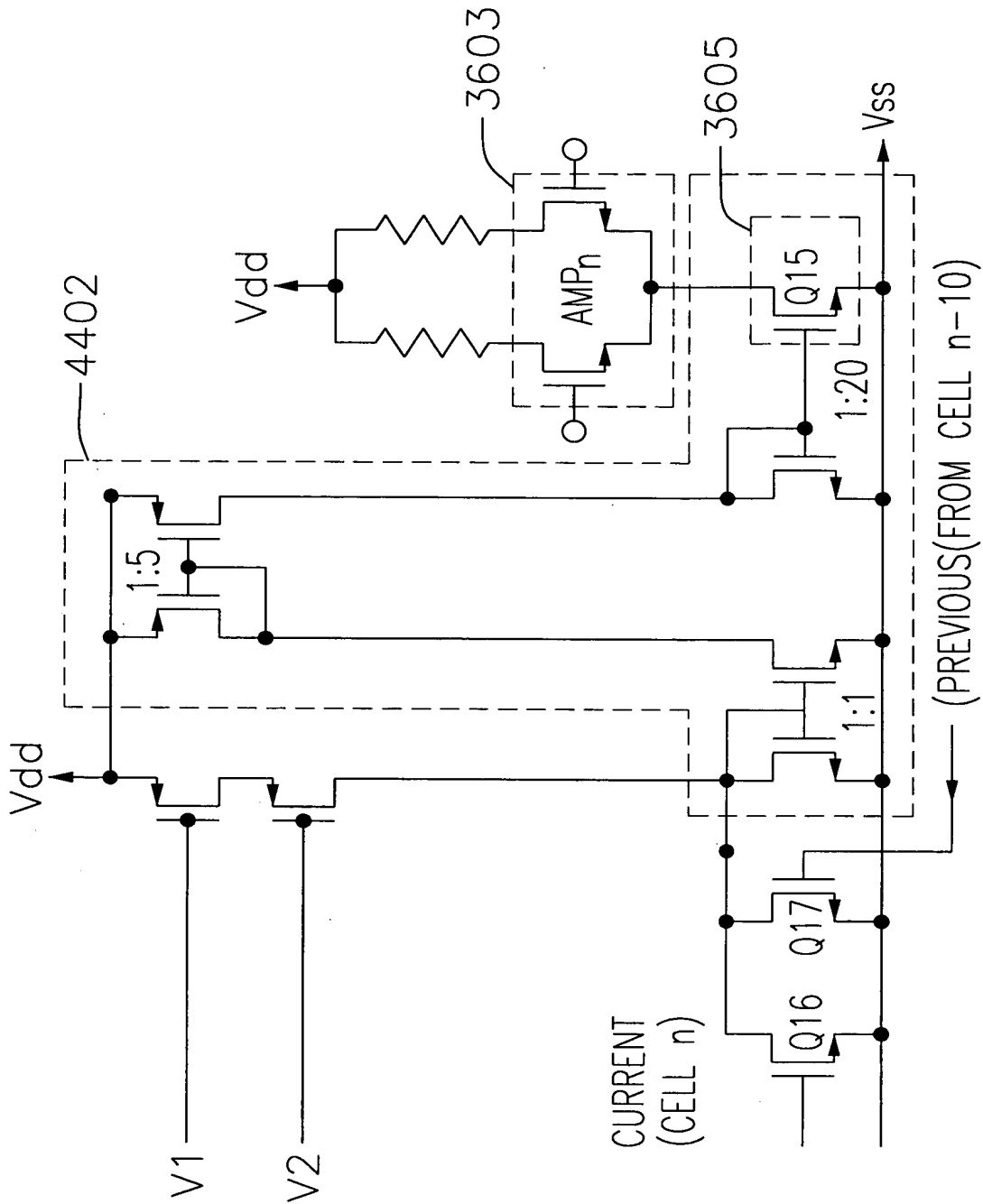


FIG. 45

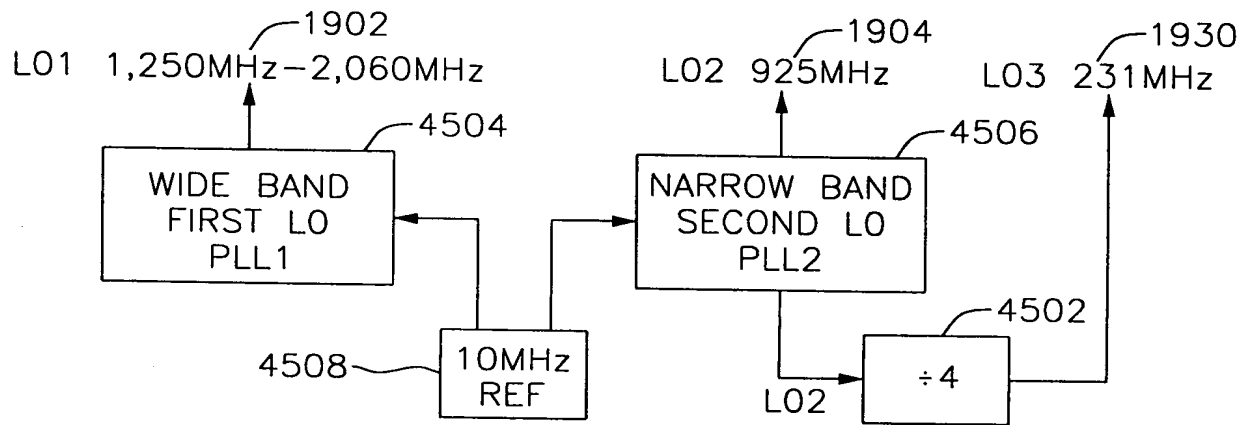


FIG. 46

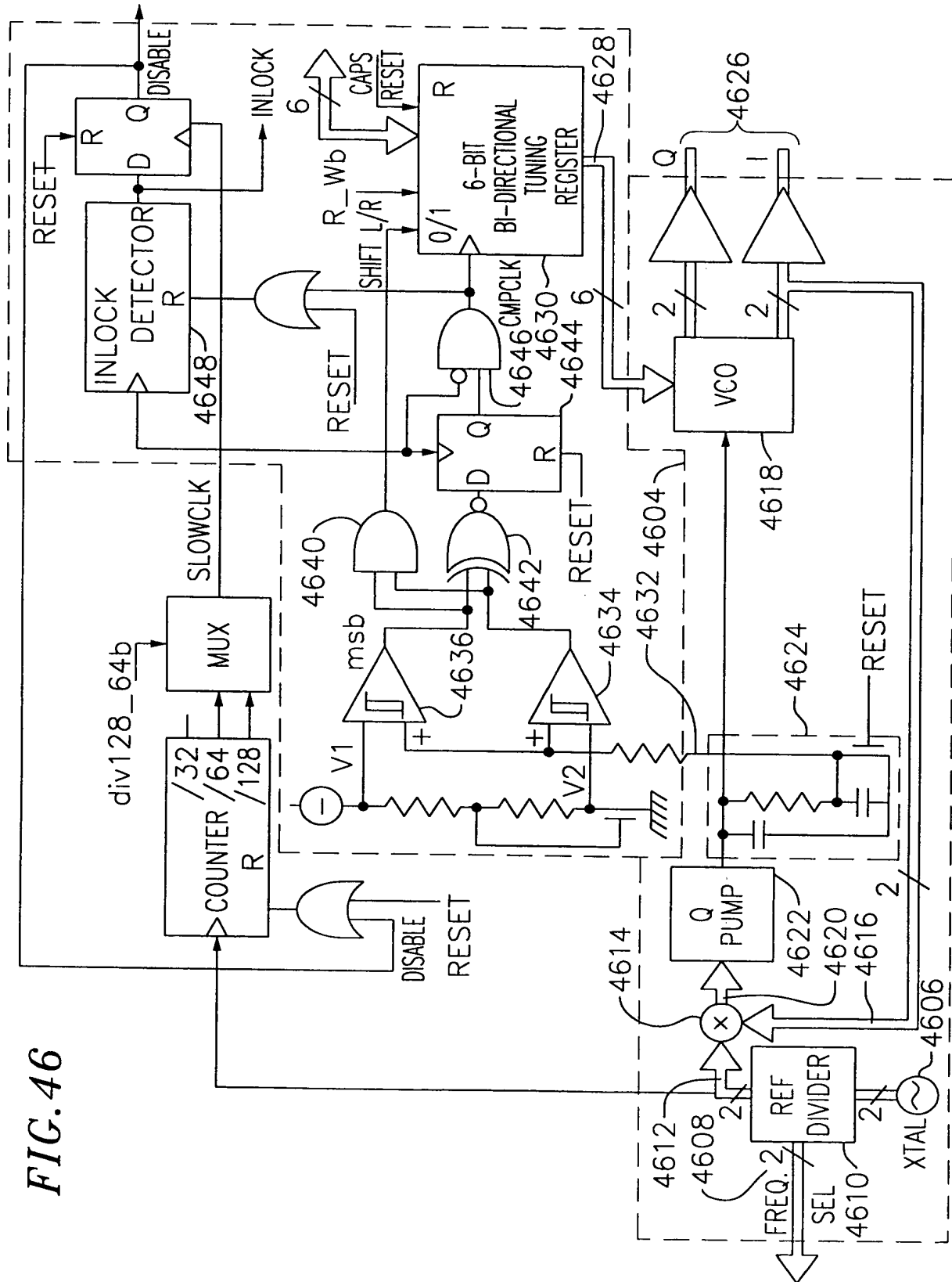
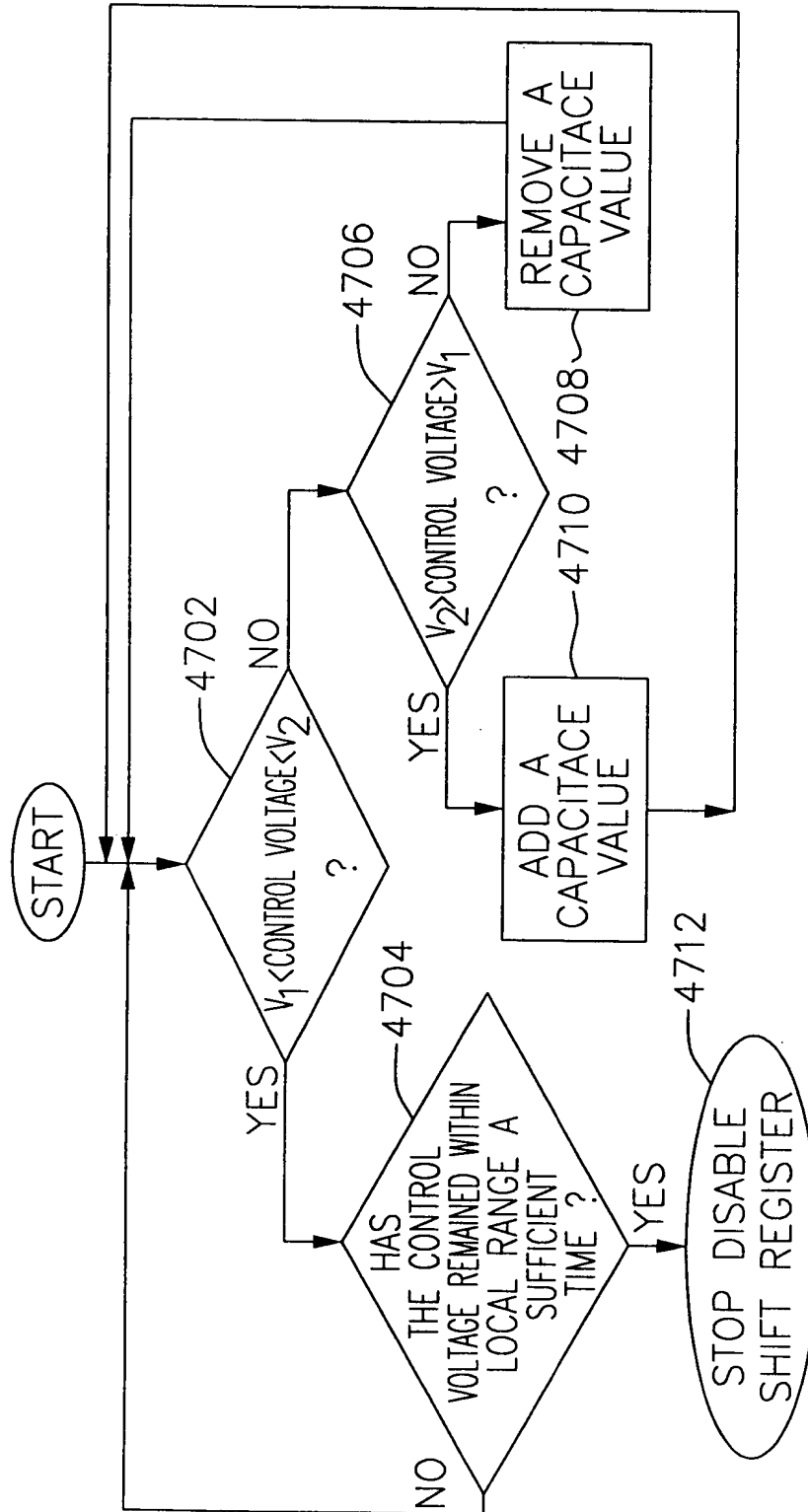


FIG. 47



EXTERNAL 36 OR 44MHz FILTER OPTION
E.G. SIEMENS X6964 (fc=43.75MHz)

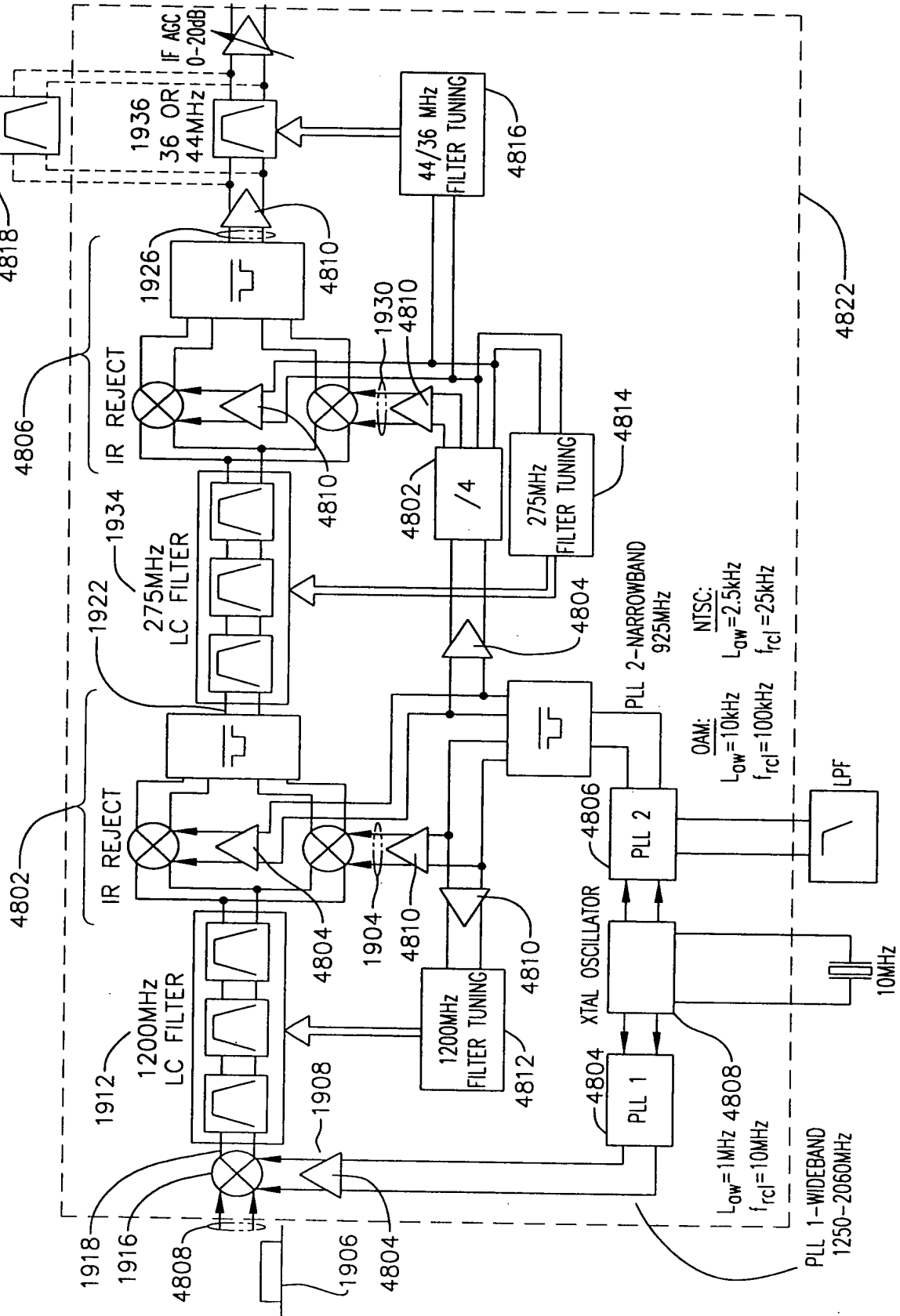
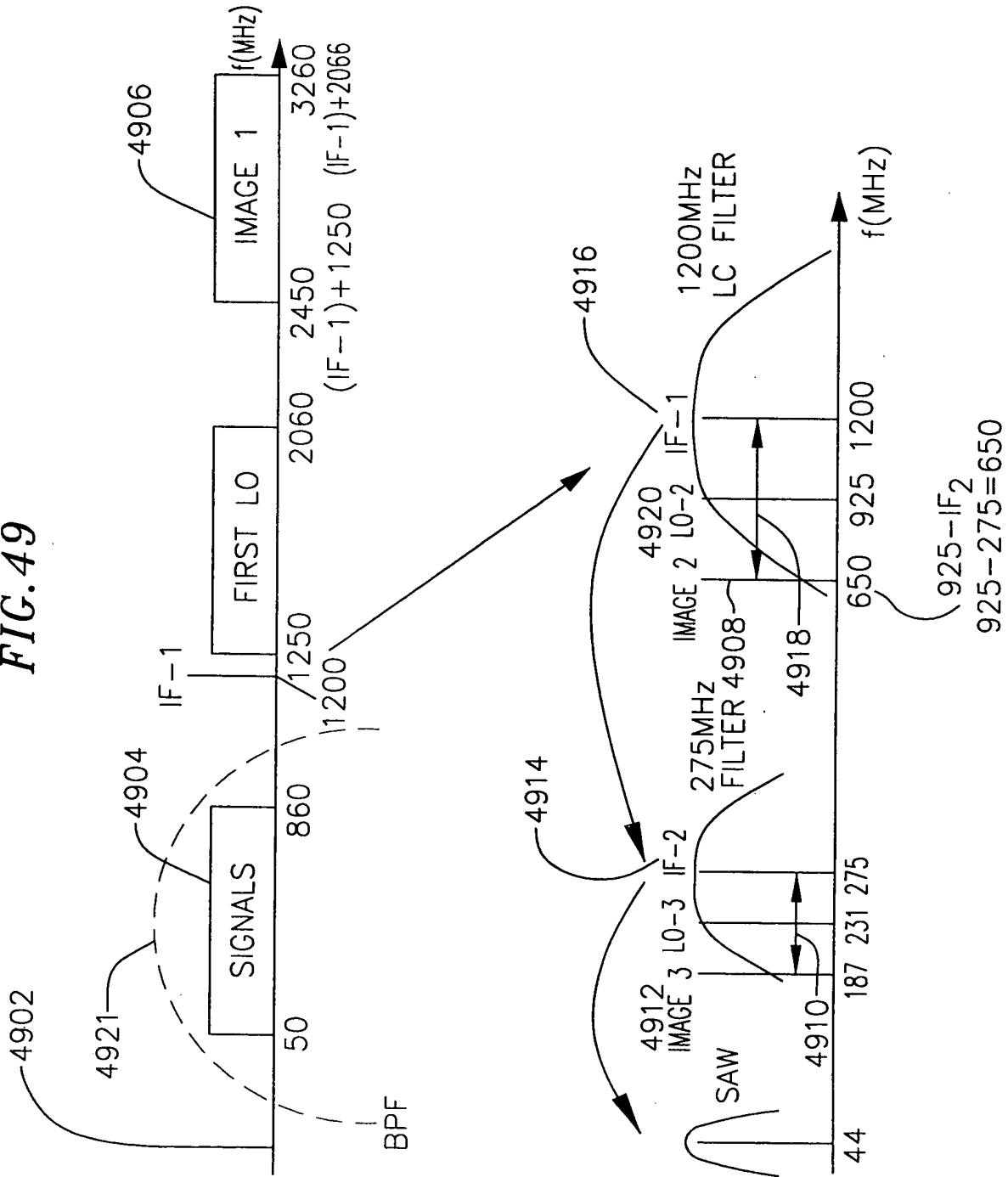
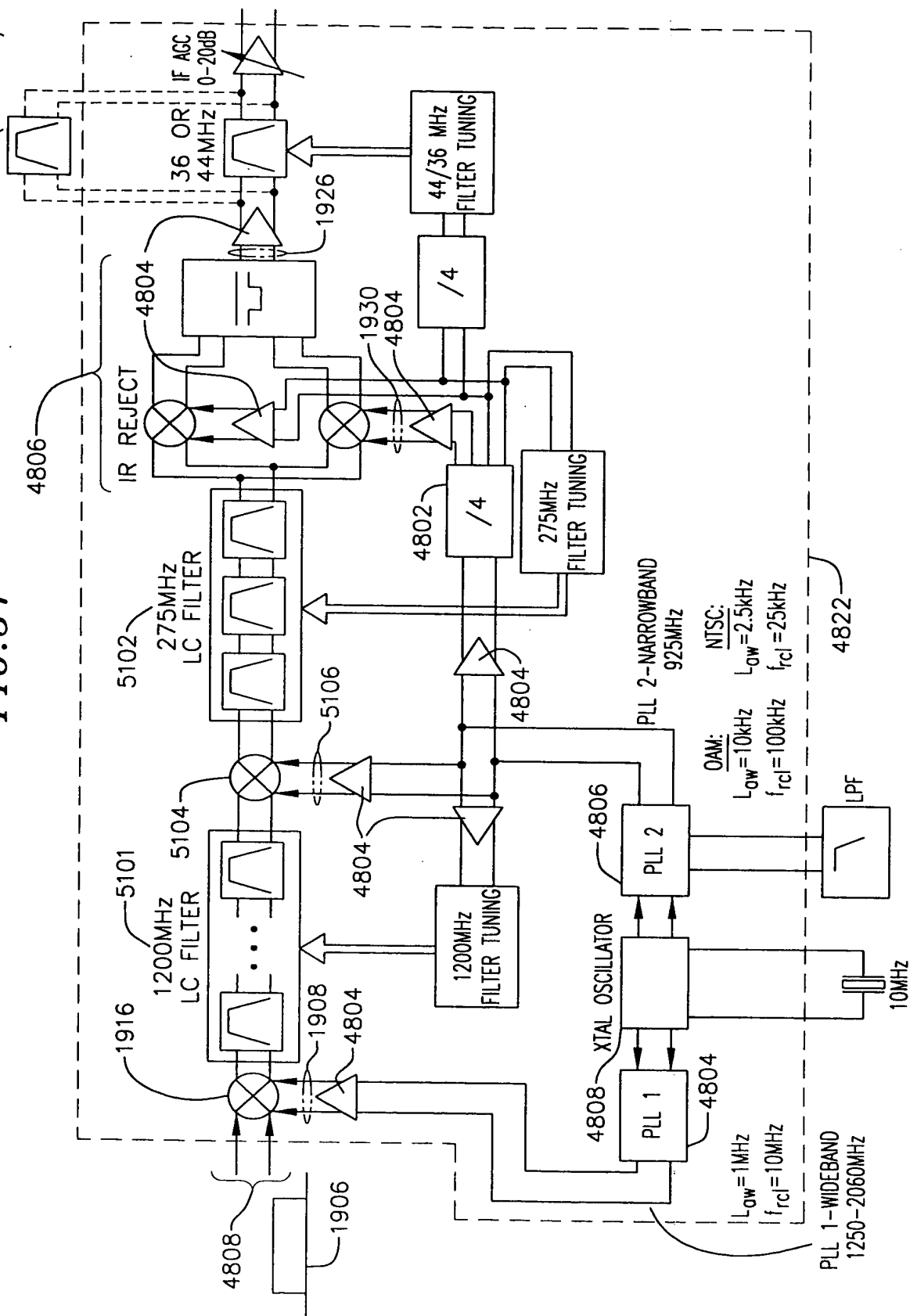


FIG. 49



The diagram illustrates a PLL system. An input signal f_{RF} (4510) is split into two paths. One path goes through a 90 DEGREES phase shifter (5006) to a multiplier (5002). The other path goes through a PHASE SHIFT NETWORK (5008) to a multiplier (5004). The PHASE SHIFT NETWORK (5008) also receives a feedback signal f_{LOI} (4512) and produces a signal Q . The output of the multiplier (5002) is $(f_{RF} + f_{LOI})$ (4520). The output of the multiplier (5004) is $(f_{RF} - f_{LOI})$ (4516). These two signals are summed at a summing junction (+) (4514) to produce the final output f_{RF} (4510).

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G. SIEMENS X6964 (fc=43.75MHz)



EXTERNAL 36 OR 44MHz FILTER OPTION
 E.C.SIEMENS X6964(f_c=43.75MHz)

FIG.52

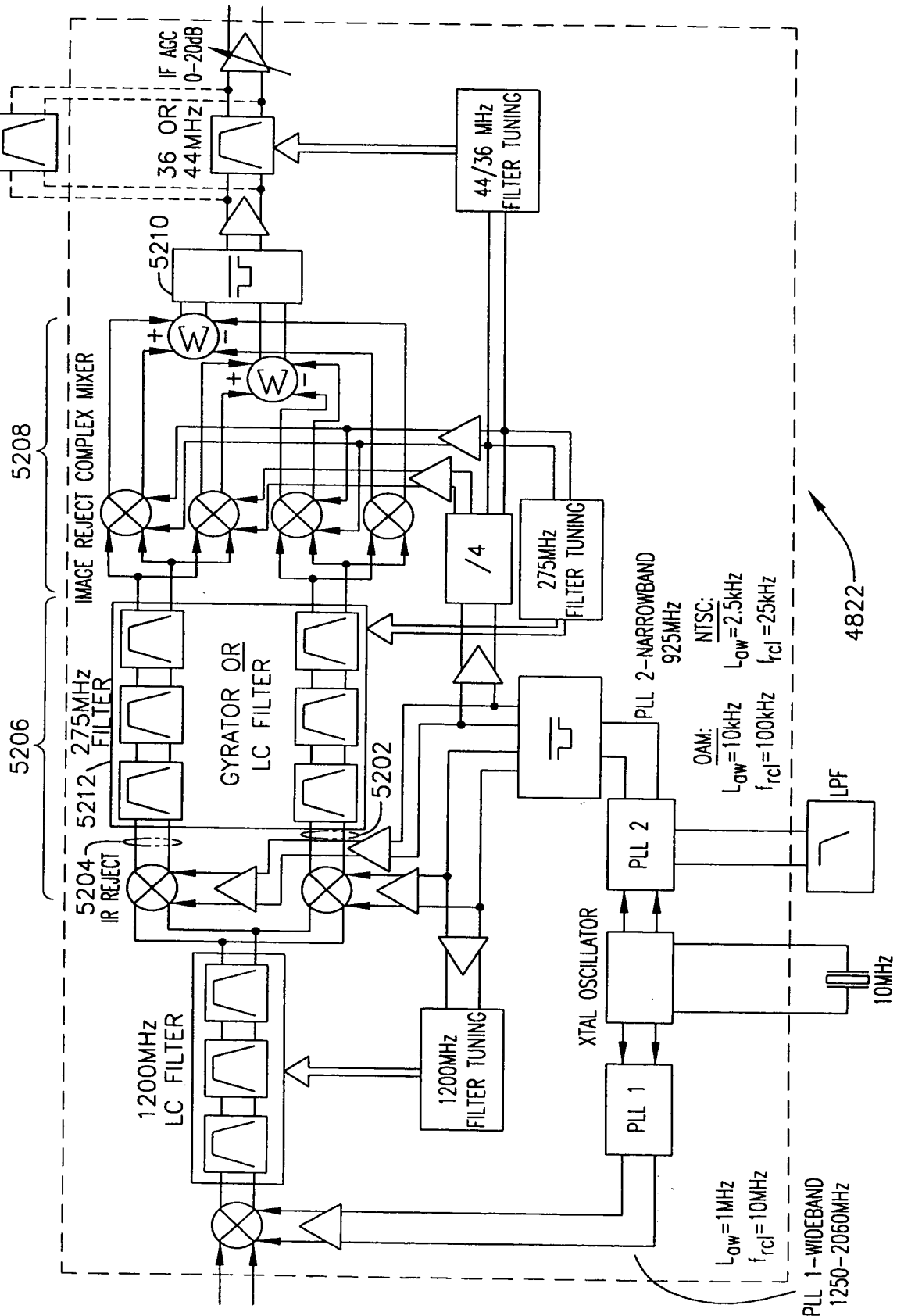


FIG. 53
 CATV TUNER

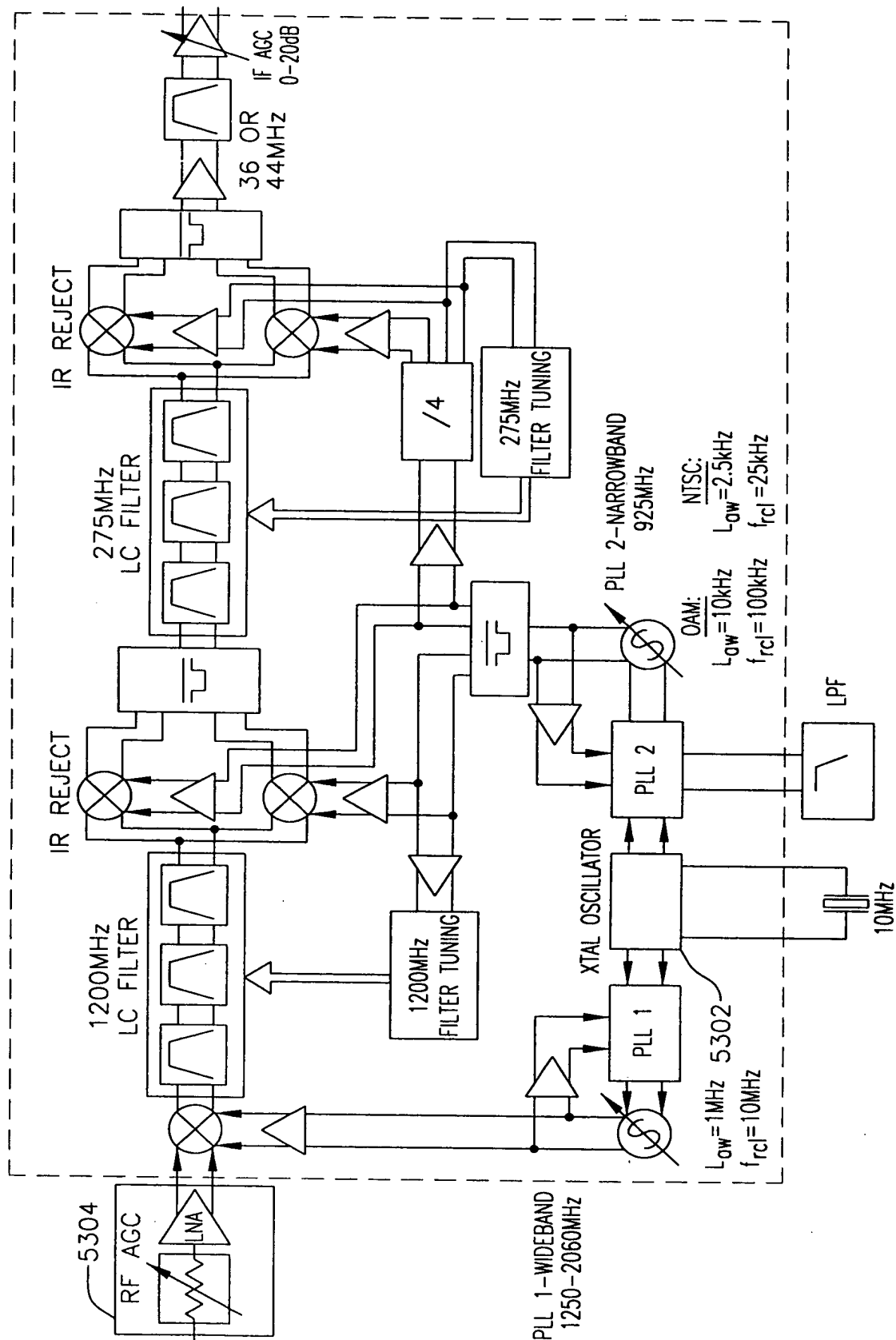
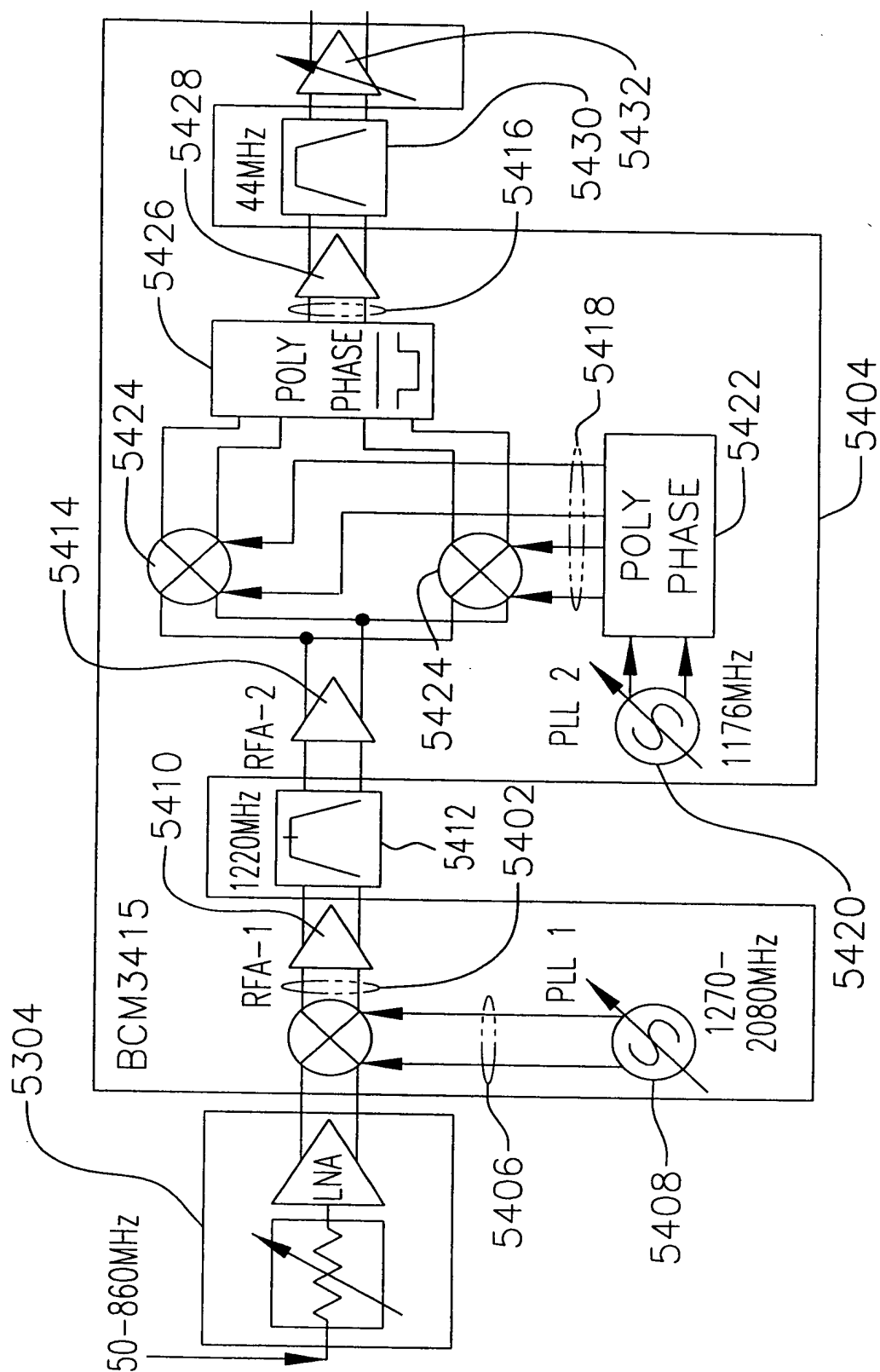


FIG. 54



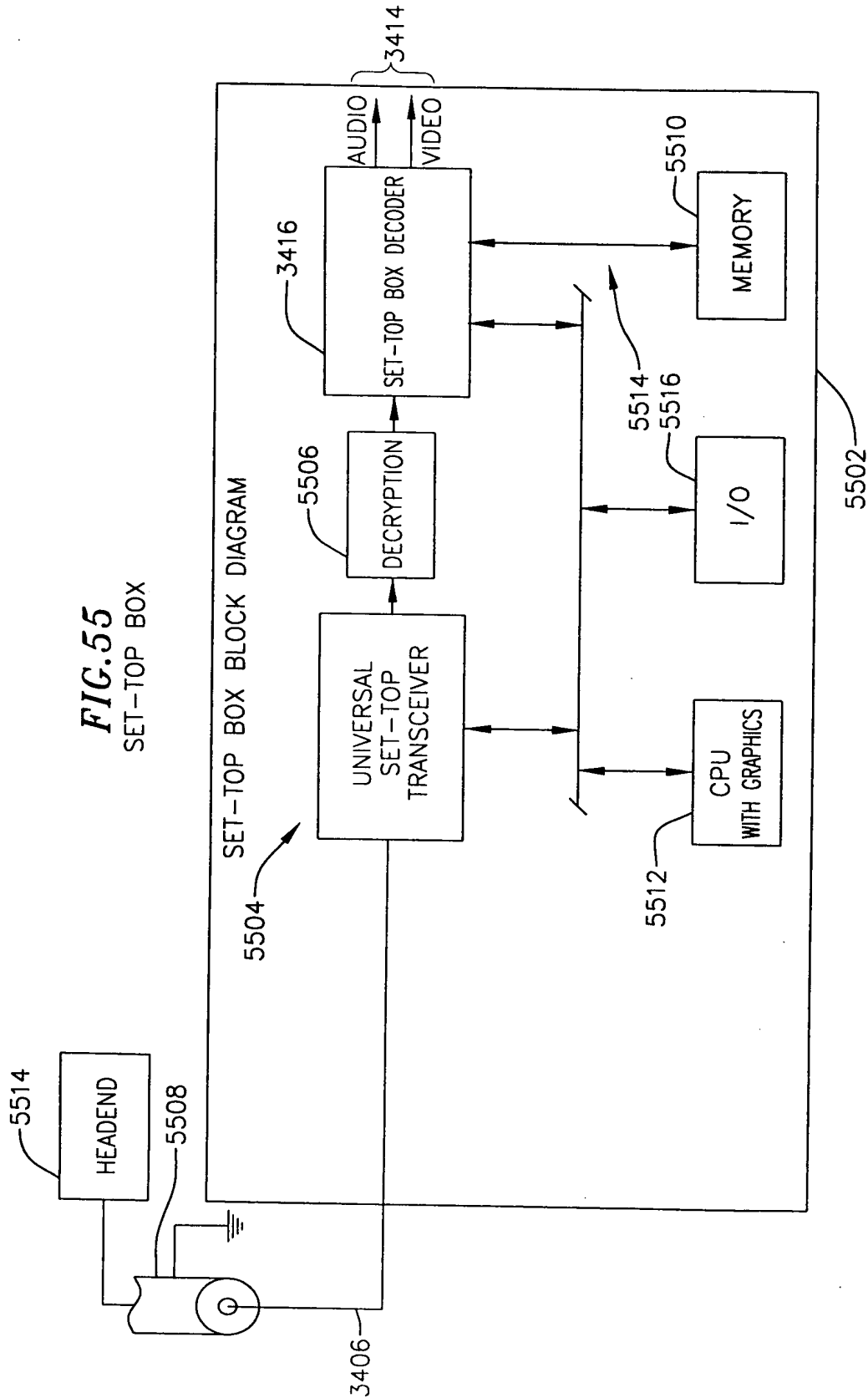


FIG. 56

TELEVISION

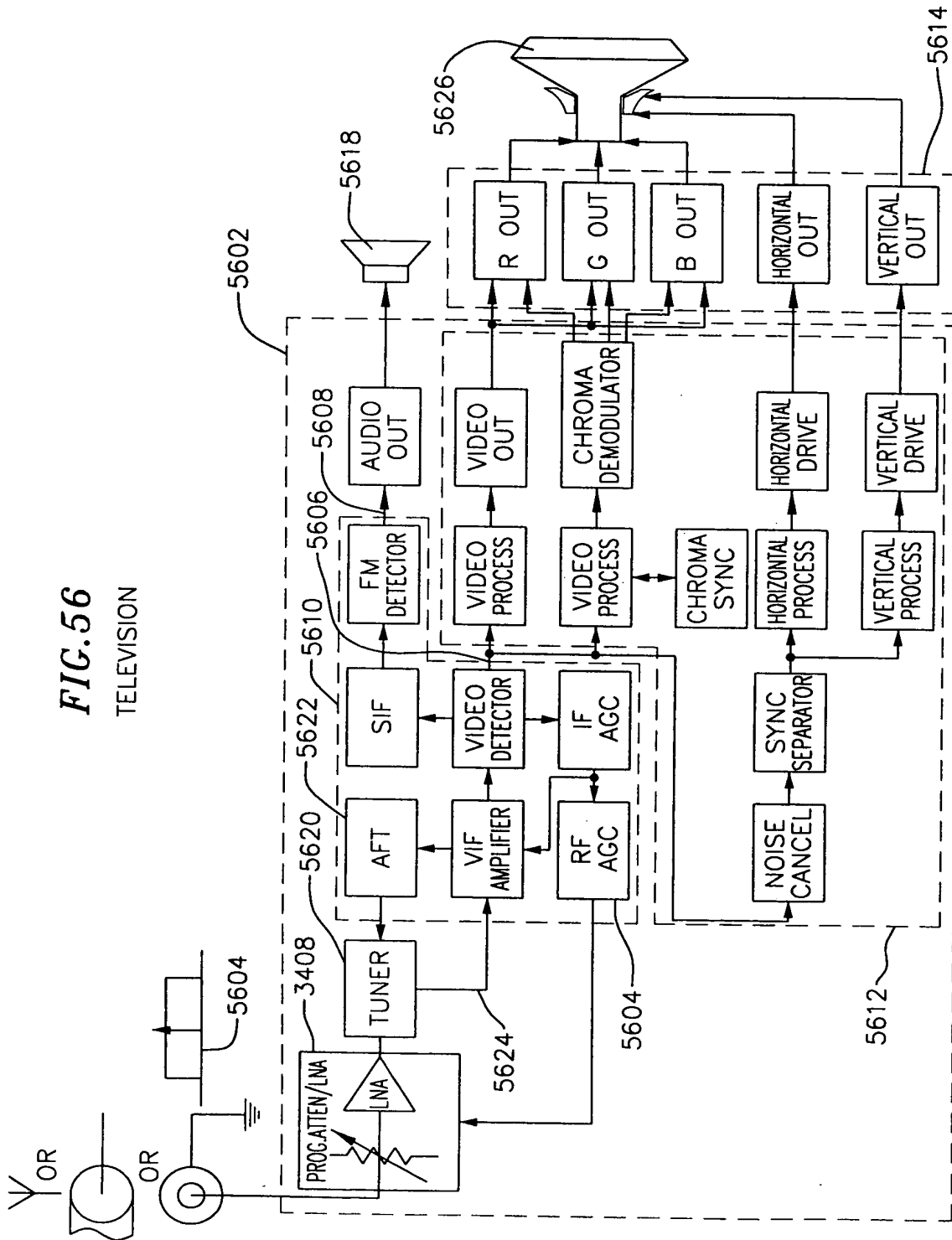


FIG. 57
 VCR BLOCK DIAGRAM

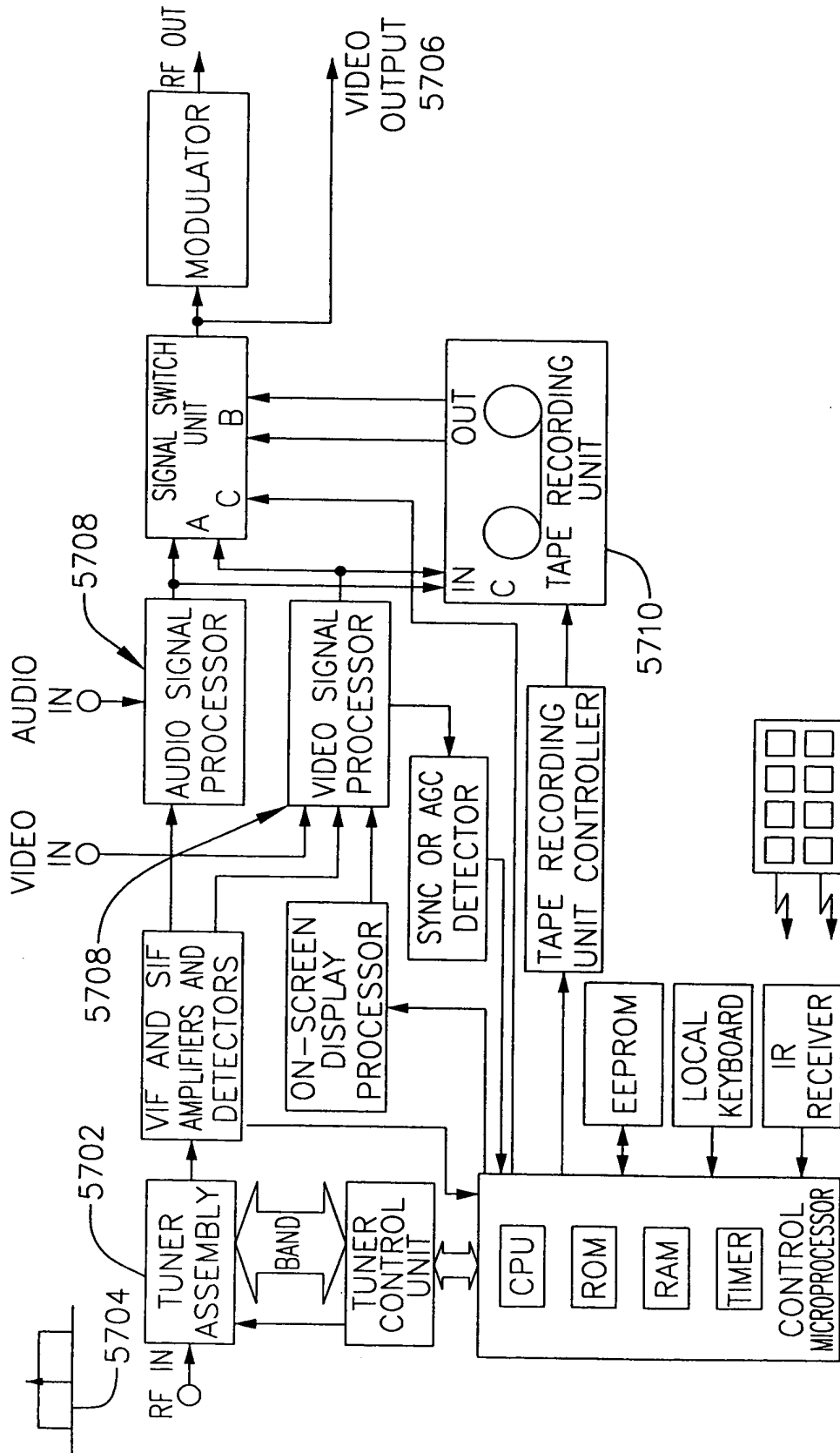


FIG. 58

